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Application Note

OPERATIONAL ASPECTS OF MOTOROLA'S DATA TERMINAL TRANSMITTER AND RECEIVER

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The MC2257, MC2259, and MC2260 are special MOS LSI devices that perform various functions relating to the transmission of digital data information in data terminal applications. This application note provides an in-depth discussion of the operation of these parts.
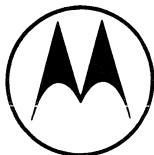
MOTOROLA Semiconductor Products Inc.

OPERATIONAL ASPECTS OF MOTOROLA'S DATA TERMINAL TRANSMITTER AND RECEIVER

Data communications often entails transmission over a telephone line or other similar communications link. Data used at the transmitting and receiving ends of the single-line are generally in a parallel form for normal data handling. To transmit and receive the data over a serial communication line necessitates converting the parallel data at the transmitting end to a serial form and the opposite transformation at the receiving end. There is a standard format for data transmitted over a communications line in both asynchronous or synchronous modes

and the characteristics of these modes will be described later in the text. The asynchronous mode is adaptive to slow speed systems whereas the synchronous mode is usually used in systems with a high speed requirement. A slow speed system usually operates below 1200 baud which can be found where data is transmitted from a human interface such as a keyboard.(The MC2257, MC2259, and MC2260 have a maximum rate of operation of 200 k baud).

The overall picture of a typical data communications system is shown in Figure 1. It consists of a central com-
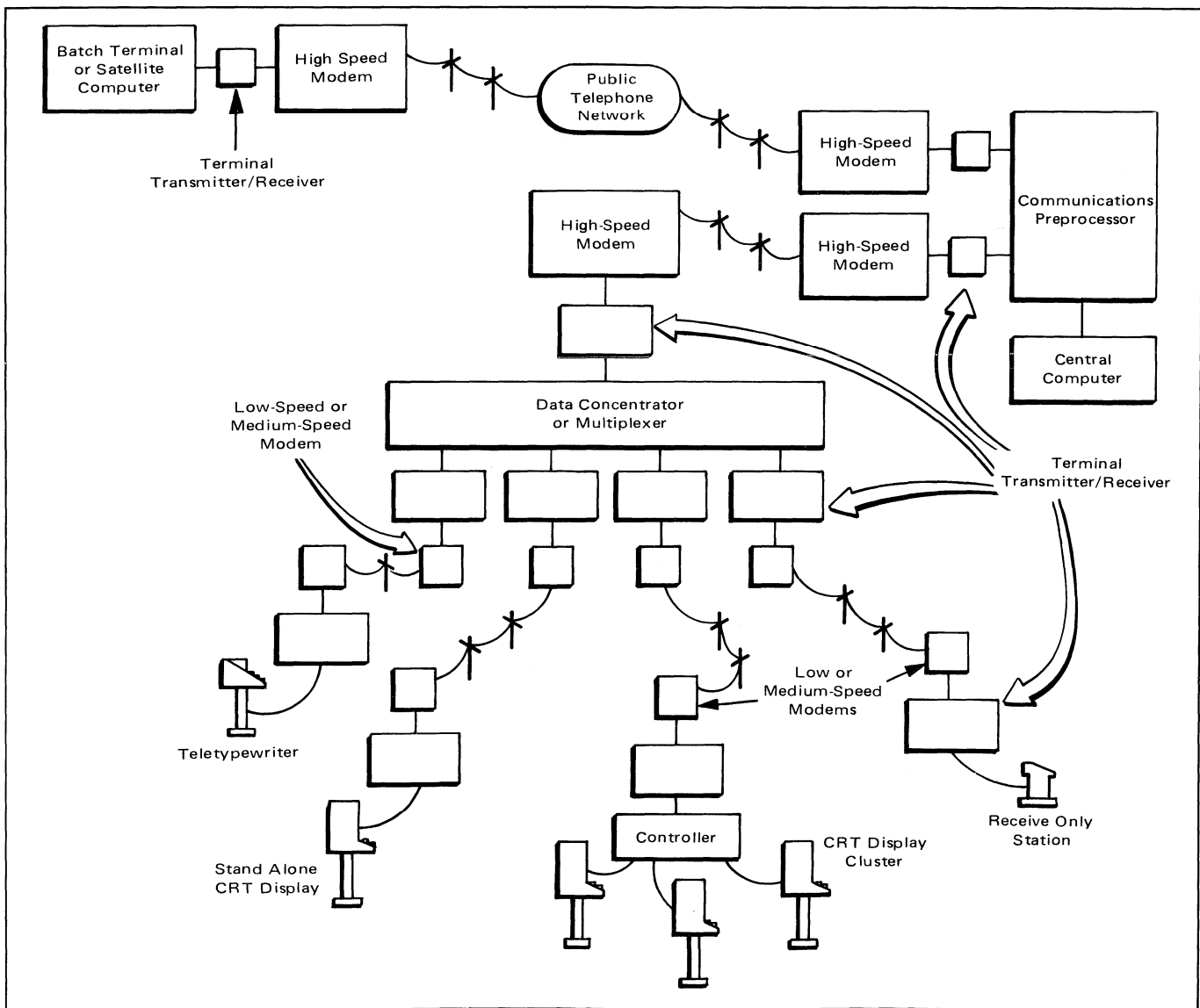

FIGURE 1 — Data Communications System and Equipment

puter receiving data from several different sources. The high speed and low speed requirements are both depicted in this figure. A data concentrator, for example, generally operates at a higher data rate than a teletypewriter and would therefore normally operate in the synchronous mode. The actual interface to the communications line in this system is a data terminal similar to that shown in Figure 2. A typical data terminal consists of a modem, a longitudinal parity checker, a bit rate generator, and a transmitter and receiver. The Data Access Arrangement (DAA) is a line adapter required by the telephone company. The incoming modulated data is converted to serial digital form by the modem. The serial data is then converted to parallel form by the terminal receiver for normal data handling at the receiving equipment. Likewise, data can be converted from parallel to serial form by the terminal transmitter and modulated by the modem to be transmitted over the telephone line. The bit rate generator provides the different external clock frequencies

The input/output timing and control logic handle the supervisory functions.

The vertical parity logic generates word parity in the transmitting mode and checks word parity in the receiving mode.

This application note will discuss the function and operation of the MC2257, MC2259, and MC2260 circuits in detail.

TERMINAL TRANSMITTER (MC2257 and MC2260)

The terminal transmitter can operate in either the asynchronous or synchronous mode. A general explanation of the operation of the transmitter in these modes will be followed by the definitions of the input and output functions of the transmitter. Then, an explanation with reference to timing diagrams will be discussed on both modes of operation.

In the asynchronous mode, the terminal transmitter will maintain an output condition of continuous "marks"
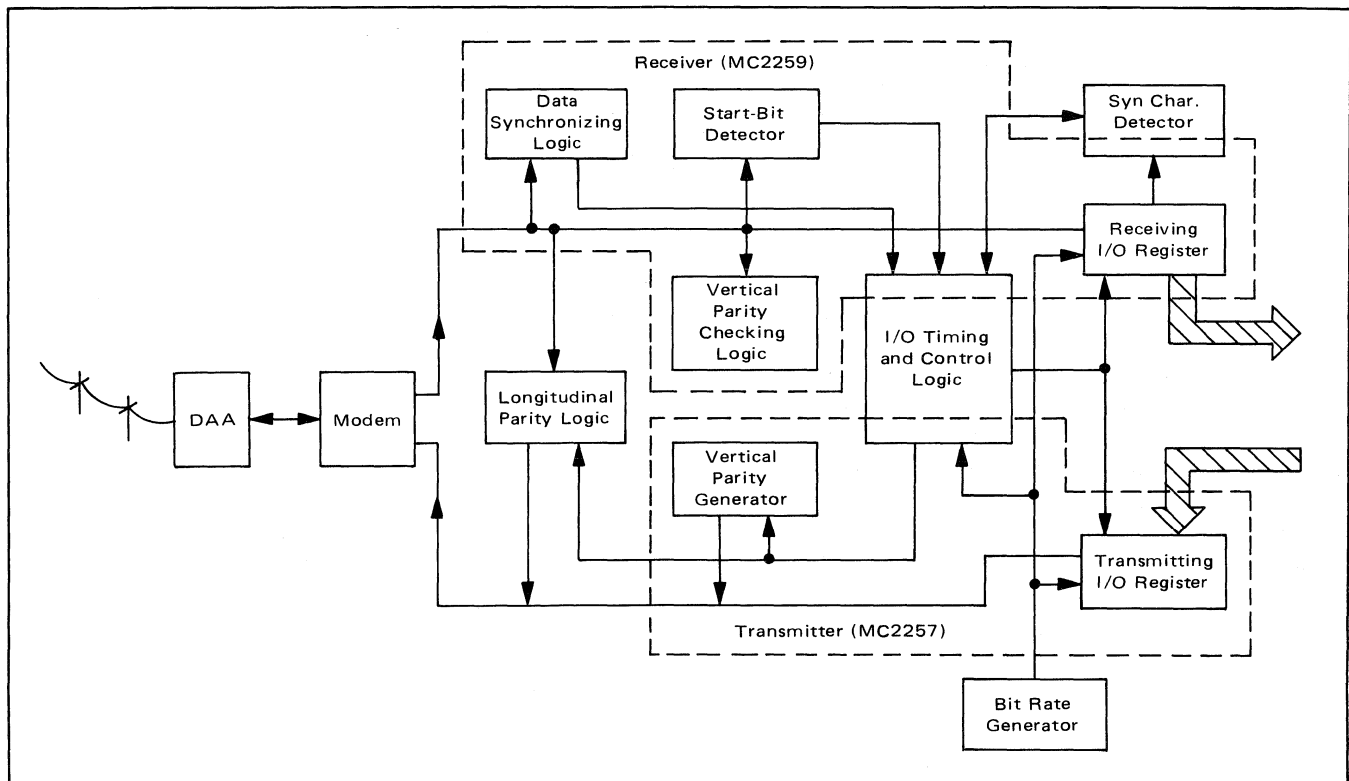
FIGURE 2 — Typical Data Terminal

required by the terminal. The longitudinal parity function generates a check character from the characteristics of the data being transmitted.

As indicated in Figure 2, the transmitter and receiver consist of several different functions. The MC2257 and MC2260 terminal transmitters, and the MC2259 terminal receiver are LSI integrated circuits which comprise the following functions:

The input/output transmitting and receiving registers perform the parallel to serial and serial to parallel conversion.

(logic "1") between the transmission of characters. The reset signal will force the transmitter into this mode of operation for a minimum of one character period. This state may be termed the "idling condition."

Data may be in the form of a character whose data bit length can range between 5 and 8 bits. If used, parity is included in the total number of bits making up the character. This data is loaded into the transmitter's buffer register and then transferred to an internal shift register.

The character transferred to the shift register will be automatically preceded by a "start bit" (logic "0") and,

then is serially transmitted to the modem at the programmed bit rate. An internal timing counter keeping track of the character position in the shift register, provides timing control to the sequence control logic which inserts parity (if utilized) into the last bit position of the character, and adds the "stop bit/s". The characteristics of this format are shown in Figure 3. When transmission of a character is complete, the sequence control logic will either return the transmitter to the "idling condition" or begin a new cycle automatically if a new character has been strobed into the buffer register.

In the synchronous mode, the transmitted characters have no control bits ("start and stop" bit/s) and each character is followed immediately by another character or a character length of all "marks" if no character is being transmitted. The all "mark" character ("idling") maintains character synchronization in the receiver. The rest of the synchronous operation is identical to the asynchronous operation.

Load Strobe — A high level on the Load Strobe transfers the input character on the Data Inputs into the Storage Buffer latches and resets the Buffer Empty output. Data must not be loaded during the internal transfer time in the synchronous mode because it may result in erroneous transmission.

External Clock — This is the oscillator input that controls the transmission rate of the Terminal Transmitter. The maximum frequency of the external clock is 640 kHz in the $\div 16$ and 64 modes, and 200 kHz in the $\div 1$ mode. This enables the transmitter to operate at a maximum baud rate of 40 k baud ($\div 16$), 10 k baud ($\div 64$), and 200 k baud ($\div 1$).

$\div 16$ and $\div 64$ Counter Enables — These two Enable inputs provide a master reset capability and a means of operating the external clock frequency at 1, 16, or 64 times the bit rate.


```
| Start | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | Stop | Stop |
```

Start Bit — "Space" — Logic Zero
Stop Bits — "Mark" — Logic One
Idling Bits — "Mark"
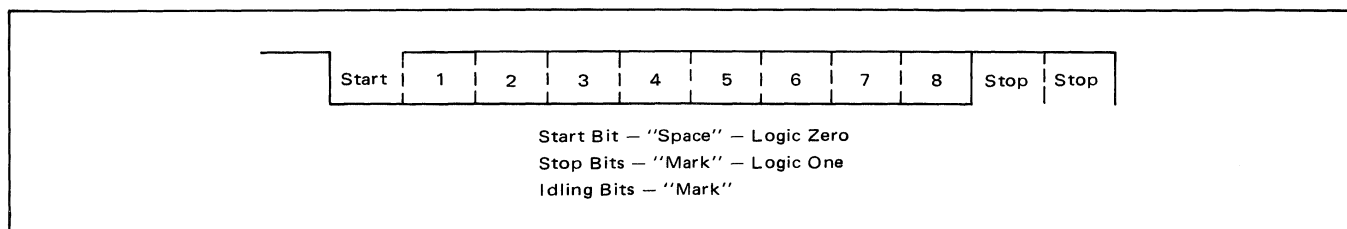
FIGURE 3 — Asynchronous Characters

TRANSMITTER I/O

The inputs and outputs of the transmitter are indicated in Figure 4. The definitions for each input and output are:

Data Inputs (D1-D8) — Characters of differing bit lengths (from 5 to 8 bits including parity bit, if desired) may be entered in parallel in right-justified bit positions by means of the eight Data Inputs. The data is strobed into a set of buffer latches where it is stored until transmitted. For proper operation, unused Data Inputs must be maintained in the high state; this can be achieved by tying unused inputs to a logic "1" source or letting the inputs float. There is no inversion of the data within the circuit; therefore, a high input will be transmitted as a logical "one".

$\div 16$	$\div 64$	Oscillator Frequency at the External Clock Input
0	0	= Bit Rate ($\div 1$)
1	0	= 16 x Bit Rate
0	1	= 64 x Bit Rate
1	1	Master Reset*

*A typical design of the external system is such that one of the divider enables is selected for the applicable external clock frequency. The other enable input then becomes a Master Reset for the Terminal Transmitter. These inputs may be changed during the idling time.

Word Length Selector — Two inputs (W_{LX}, W_{LY}) are provided to define the character bit length. The following truth table defines the character length for each

FIGURE 4 — MC2257 (MC2260) Block Diagram

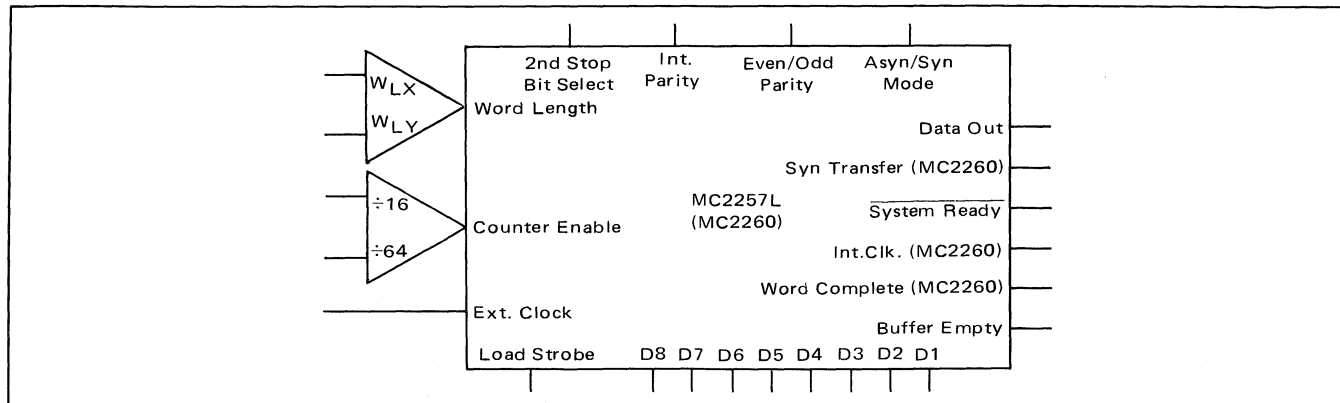input combination. (Unused Data Inputs must be maintained in the high state, which may be accomplished by leaving the unused inputs open.) This input may be changed any time except during the internal transfer time and the change becomes effective for the next character.

W_{LX}	W_{LY}	Word Length (Including parity, if applicable)
1	1	8 bits
0	1	7 bits
1	0	6 bits
0	0	5 bits

A high level is defined as a positive logic "1".

2nd Stop Bit Select (Asynchronous Mode Only) — A high level on the 2nd Stop Bit Select input causes two STOP bits to be transmitted. A low level will cause one STOP bit to be transmitted. This function is internally disabled during the synchronous mode of operation. This input can be changed any time during the character time except during the internal transfer time and the change becomes effective for the next character time.

Internal Parity — A high level applied to the Internal Parity input causes the transmitter Parity Generator to replace the trailing bit of a character of any selected word length with an internally generated parity bit. A low level causes the trailing bit to be transmitted as loaded from the inputs. This input can be changed any time during the character time except during the last data bit (parity bit) position. A high on this input prior to the transmission of the last data bit (parity bit) will cause internal parity to be included in that character.

Even/Odd Parity — When a high level is applied to both the Internal Parity and the Even/Odd Parity inputs, the Parity Generator places the proper bit value in the trailing bit position of a character to insure that the total number of high level character bits is even. Odd parity is formed by using a low level on the Even/Odd Parity input. This Even/Odd input can be changed any time during the character time except during the last data bit (parity bit) position.

Asynchronous/Synchronous Mode — A high level on the Asynchronous/Synchronous Mode input enables the device for operation in the asynchronous mode. A high level also causes the generation of START and STOP bits, and causes MARK bits to appear on the Data output terminal between the transmission of characters without control bits (START, STOP). It also provides automatic recycling to either transmit the next data character or a character length of MARK bits to maintain synchronization. This input may be changed during the idling time or master reset time.

Data Output — This output transmits serial data of the information presented in parallel form for a character. Start and stop bits as well as a parity bit may be included if the device has been conditioned to provide such information.

Syn Transfer (MC2260) — This output goes high for the last two bits of a synchronous character. It provides an indicator for sync character loading one bit time prior to the transfer time. Also, it provides an indicator for preventing an improper change of the 2nd stop bit and word length selector inputs. The transfer time occurs at the approximate midpoint of the Syn Transfer pulse.

$\overline{\text{System Ready}}$ (Asynchronous Mode only) — This input allows control of the transmitter by the external system. A low level releases the transmitter for the next transmission cycle. This signal is normally applied after the Buffer Register has been loaded (Buffer Empty output is low). The low level should be maintained until the next transmission cycle is initiated (the Buffer Empty output goes high), then held high until after the next Data Strobe has occurred. In a typical application the $\overline{\text{Buffer Empty}}$ output may be tied directly to the $\overline{\text{System Ready}}$ input.

Internal Clock (MC2260) — The internal clock that is generated at the data bit rate is available for external use from this output. For example, the equipment of which the transmitter is a part, may require a clock source that has a frequency equivalent to the data rate of the transmitter.

Word Complete (MC2260) — In the Asynchronous mode, the Word Complete output is generated during the last stop bit time and remains "high" if the transmitter returns to an idling condition. In the synchronous mode, the Word Complete output is generated during the last bit time of a data or idle character. The word complete output defines the end of a character time which indicates to another transmitting source that it may transmit.

Buffer Empty — A high level on the Buffer Empty output indicates that the data previously stored in the Buffer Storage latches has been transferred into the Shift Register and the latches are available for new data. The Load Strobe input automatically resets this output during the load cycle.

ASYNCHRONOUS OPERATION

Each character is transmitted as a non-return to zero (NRZ) waveform at the programmed bit rate. This transmission format is illustrated in the second row of Figure 5. The internal clock signals resulting from the various external clock modes are also shown. For instance, in the divide by 16 mode, sixteen external clock pulses are required to transmit each bit as indicated in rows 6 and 7 of Figure 5. Positive transitions of the internal clock signal shift the data out of the right-justified flip-flop position of the shift register. A bit counter keeps track of the character's position in the shift register and provides timing control to the sequence control logic for the insertion of parity (if internal parity is selected) into the last bit position of the character, and adds the stop bit/s. The data transmitted from the transmitter may or may not have idling between characters depending on the system design.

The flow diagram and functional block diagram of the transmitter, Figures 6 and 7 respectively, should be used as an aid to understanding the operating sequence.

① Data Character

② NRZ Transmission Format

③ Data Bit

④ External Clock (÷1)

⑤ Internal Clock (÷1)

⑥ External Clock (÷16)

⑦ Internal Clock (÷16)

⑧ External Clock (÷64)
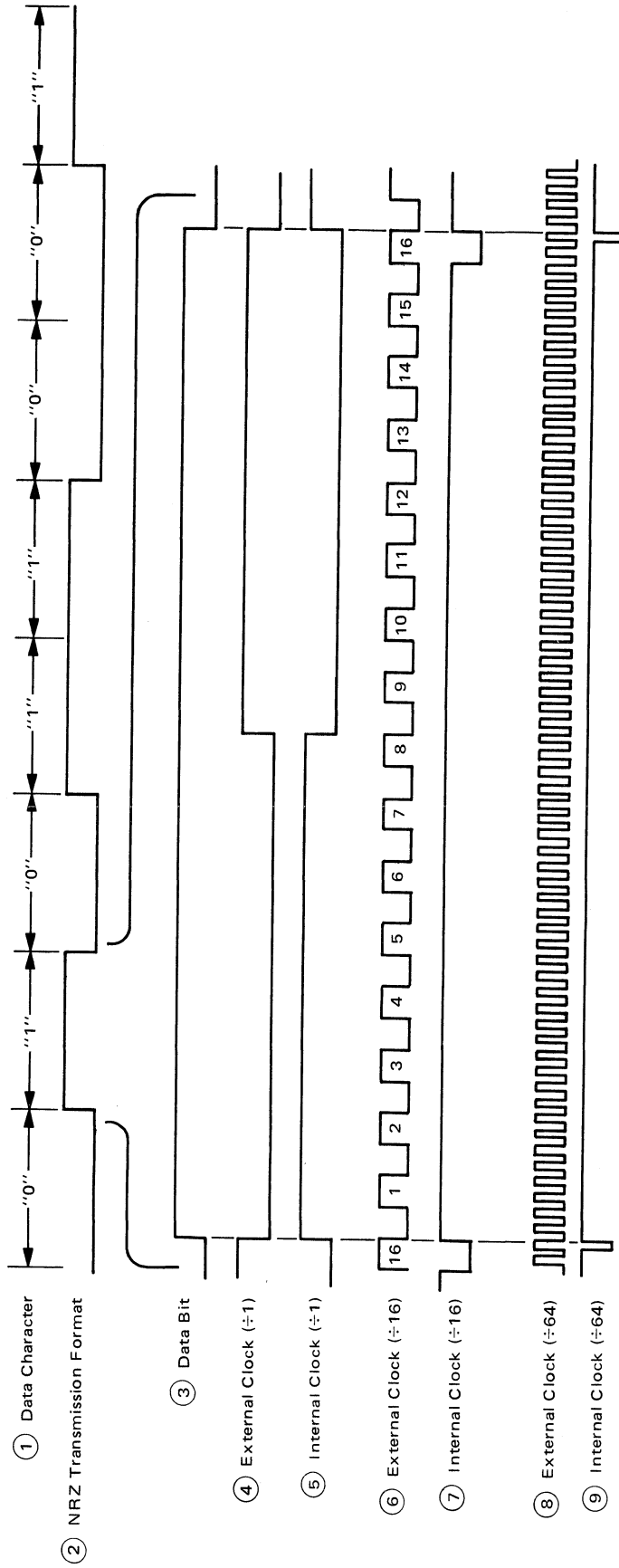
⑨ Internal Clock (÷64)

FIGURE 5 — Transmission Format and Internal Clock versus External Clock Mode

6

Start

Master Reset (÷16 Enable ● ÷64 Enable = "1"):
    Fills Shift Register with Marks ("1"s)
    Sets Buffer Empty Latch (Output = "1")
    Initializes Bit Counter
    Resets Parity Generator
    Resets Transfer Timing Logic
    Resets ÷64/÷16 Clock Counter
    Initializes Stop Bit Generator
    Inhibits Start Bit Generator
Data Output = Mark ("1")

Clock Generation Sequence

Increment Clock Generator Counter

Clock Mode ?
    64
    16

Counter = 64 ?   No
Counter = 16 ?   No

Yes   Yes

Enable Internal Clock

Shift Data in Shift Register One Bit Right
Increment Bit Counter

Bit Counter Full ?   No   Yes

Inhibit Parity Generator Output

Generate First Stop Bit

Is 2nd Stop Bit Required ?   Yes   No

Generate 2nd Stop Bit

System Ready = 0 ?   No   Yes

Place Mark On Data Output

Initialize Bit Counter
Initialize Stop Bit Register
Transfer Contents of Buffer Storage Register to Shift Register
Set Buffer Empty Latch (Output = "1")
Reset Parity Generator
Set Start Bit (Space) in Most Significant Shift Register Bit

Shift Data in Shift Register One Bit Right
Increment Bit Counter

Bit Counter Full ?   No   Yes

Generate Internal Parity ?   No   Yes

Shift Last Bit in Shift Register to Output

Replace Last Bit in Shift Register with Contents in Parity Generator
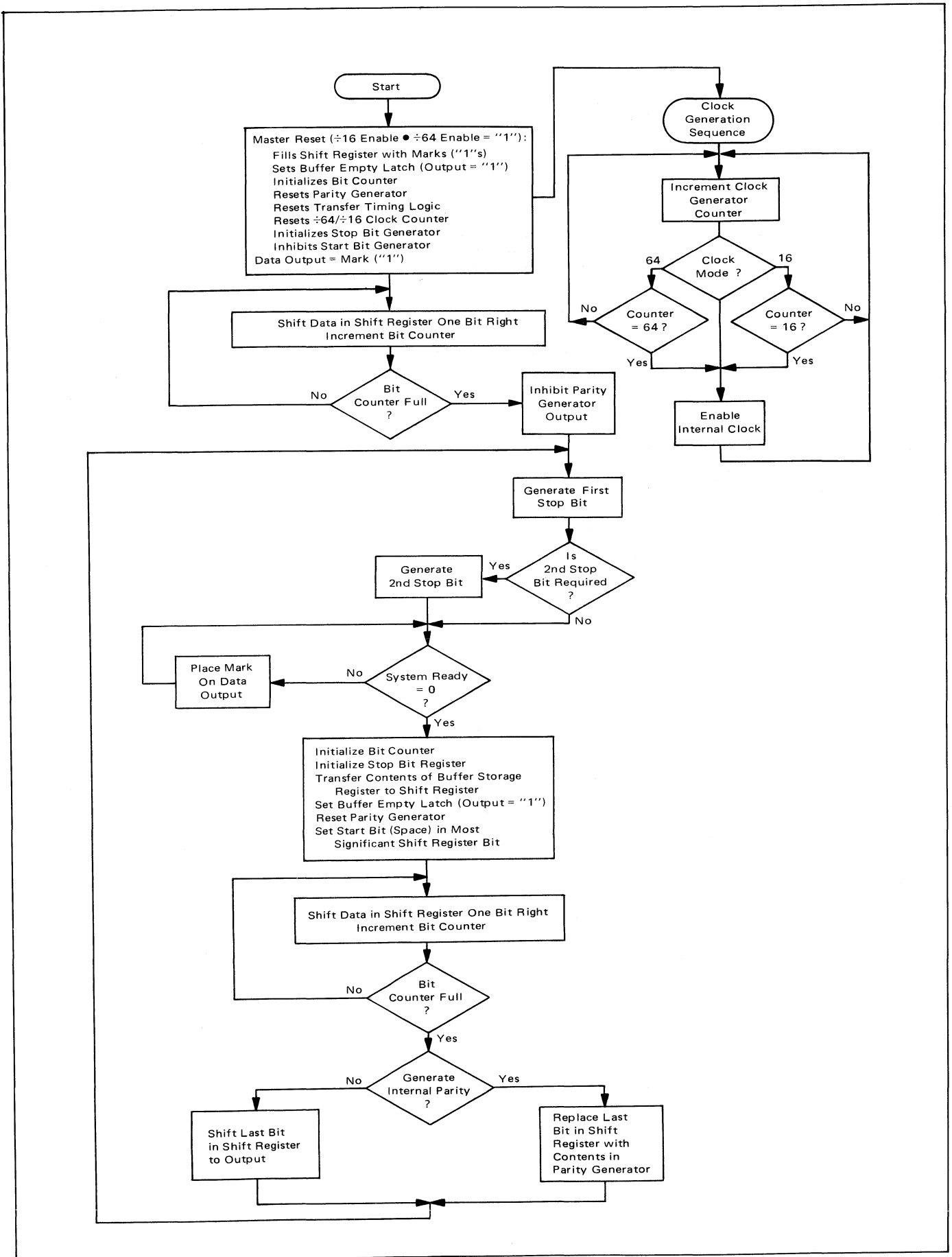
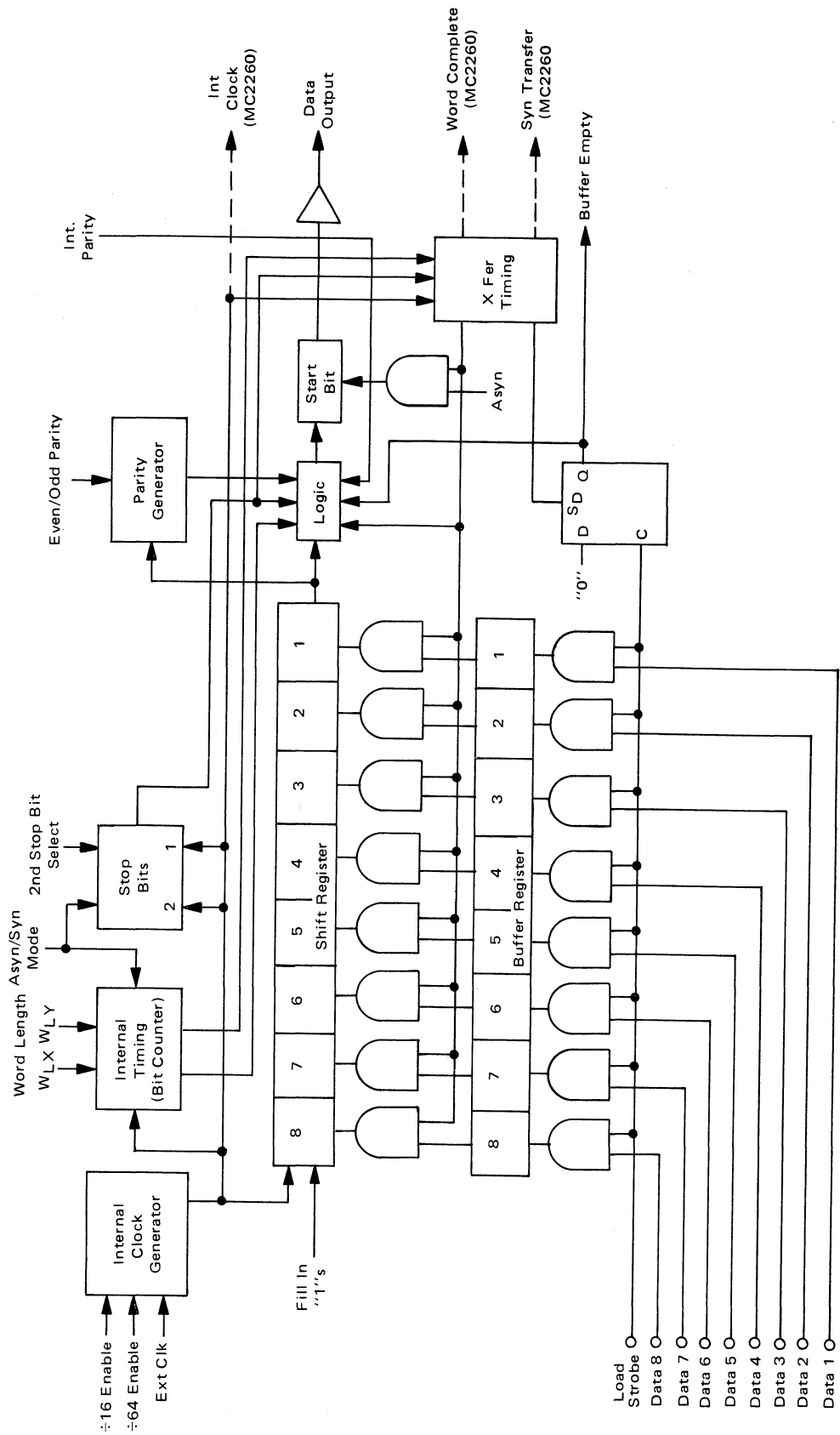FIGURE 6 — MC2257 Terminal Transmitter Asynchronous Operation Flow Diagram

7

FIGURE 7 – Terminal Transmitter (MC2257 and MC2260)

8

A master reset should be applied after power turn-on to ensure that the internal flip-flops are in the correct state. A master reset applied after power turn-on or during transmission will clear the internal bit and clock counters, fill the shift register with "1's", and cause the Buffer Empty output to go to the "high" state. At this time the Data output line is forced into the idling mode. When the master reset is released, the internal clock generator is enabled which initiates shifting and enables the bit counter. After a master reset the Data output will remain in the idling mode because of the filled "1's" until one complete character (including stop bit/s but not the start bit) has been "transmitted" as shown in Figure 8. The parity generator is inhibited at this time and a "one" is placed on the Data output in place of the parity bit.

The master reset forces the Buffer Empty output "high" indicating that data may be loaded into the buffer after reset. Data from an external source is loaded into the buffer register by means of the Data inputs when the Load Strobe input is in the "high" state. The positive transition of the Load Strobe forces the Buffer Empty

output to a "low" level indicating that the buffer register contains data. The buffer register acts as a temporary storage register which holds one character. Also, the data on the Data inputs of the buffer register is continuously reflected in the buffer register when the Load Strobe input is a high; the negative transition of the Load Strobe latches the data in the buffer register which is then impervious to any further change of the Data inputs.

An external signal can be applied to the $\overline{\text{System Ready}}$ input anytime after the Buffer Empty output goes to a logic "zero" state. When the $\overline{\text{System Ready}}$ input is "low", it is an indicator to the transmitter that data is available for transmission. However, the $\overline{\text{System Ready}}$ input has no effect on the transmitter until the stop bit/s of the previous character has been transmitted out of the shift register. Then, if the $\overline{\text{System Ready}}$ is "low", the internal transfer signal is generated which clears all functional logic except the buffer register and shift register, and subsequently automatically transfers the data in the buffer register into the shift register. The internal transfer signal that is generated at this time also causes the Buffer Empty
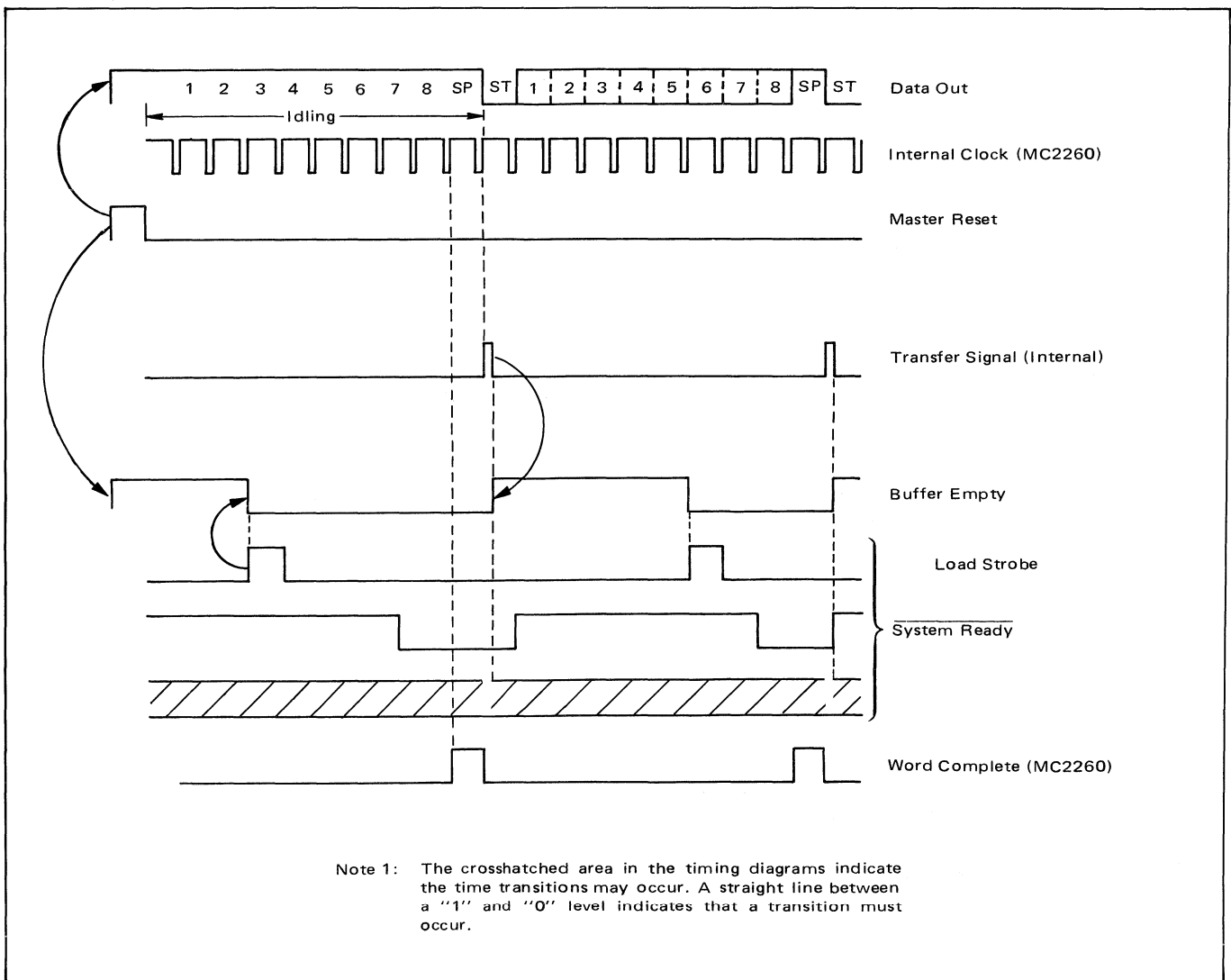

FIGURE 8 – Transmitter Asynchronous Operation
(1 Stop Bit)

output to return "high" and generates the start bit as shown in Figure 8.

The System Ready should be brought back "high" after the Buffer Empty output returns to a "high" state. If the System Ready input is "high" at the time of completion of a character's transmission, and no Load Strobe has occurred, the Serial Data output will return to the idling mode as desired. If the System Ready remains low and no Load Strobe occurs during a character time, a start bit with forced "ones" for the data bits will be transmitted. Taking the System Ready low while the transmitter is idling causes the internal transfer signal and start bit to be generated as shown in Figure 9. There are two possible ways to use the System Ready input. First, the Load Strobe and System Ready inputs provide two separate controls dependent on the state of the Buffer Empty output as previously explained; this provides a control which is independent of Load Strobe. Second, the System Ready input and Buffer Empty outputs can be tied together thereby eliminating System Ready input as a separate control.

Operationally the MC2257 and MC2260 are identical, however the MC2260 is packaged in a 28-pin package in order to provide Internal Clock, Word Complete, and Syn Transfer outputs. The Word Complete output is generated during the last stop bit time as shown in Figure 8. If there is idling after the last stop bit, the Word Complete output remains "high" for the duration of the idling time as shown in Figure 9. The Word Complete output allows the user to operate the transmitter in the full duplex or half duplex modes. (The Half Duplex mode is defined as data being transmitted over a single line in both directions but in only one direction at any given time. The Full Duplex mode is defined as data being transmitted over a single line in both directions at the same time. Data transmitted in a single direction over a single line is known as Simplex).

SYNCHRONOUS OPERATION

The synchronous operation of the transmitter is similar to the asynchronous operation with the exception that the System Ready and "2nd Stop bit select" inputs have no effect on the operation. The flow diagram for the synchronous operation is shown in Figure 10.

A master reset applied during transmission of a character or for initialization of the transmitter clears the internal counters, fills the shift register with "1's", causes the Buffer Empty output to go "high", and forces the data output line into the idling mode. Similar to the asynchronous operation, the data output will remain in the idling mode until one complete idling character has been transmitted as shown in Figure 11. The parity generator is automatically inhibited during the idling mode and a "one" is forced onto the data output in the parity bit position.

Data may be strobed into the buffer when the Buffer Empty output is "high" after reset (the unused data inputs should be left open or logically held "high"). Data on the inputs is continuously reflected in the buffer when the Load Strobe is a logic "1", and the negative transition of the Load Strobe latches the data in the buffer which is then impervious to any further change of the data inputs. Also, the positive transition of the Load Strobe resets the Buffer Empty output to a "low" level which indicates the buffer is full as shown in Figure 11. A Load Strobe pulse should not occur during the internal transfer time for proper operation. When the last bit of the previous character is transmitted and the Buffer Empty output is "low", the internal transfer timing logic automatically clears all functional logic except the buffer storage register and then causes a transfer of the data in the buffer into the shift register. Note: System Ready and the 2nd stop bit inputs have no effect on the transmitter in the synchronous mode. Then, the internal timing counter will keep track of the character position in the shift
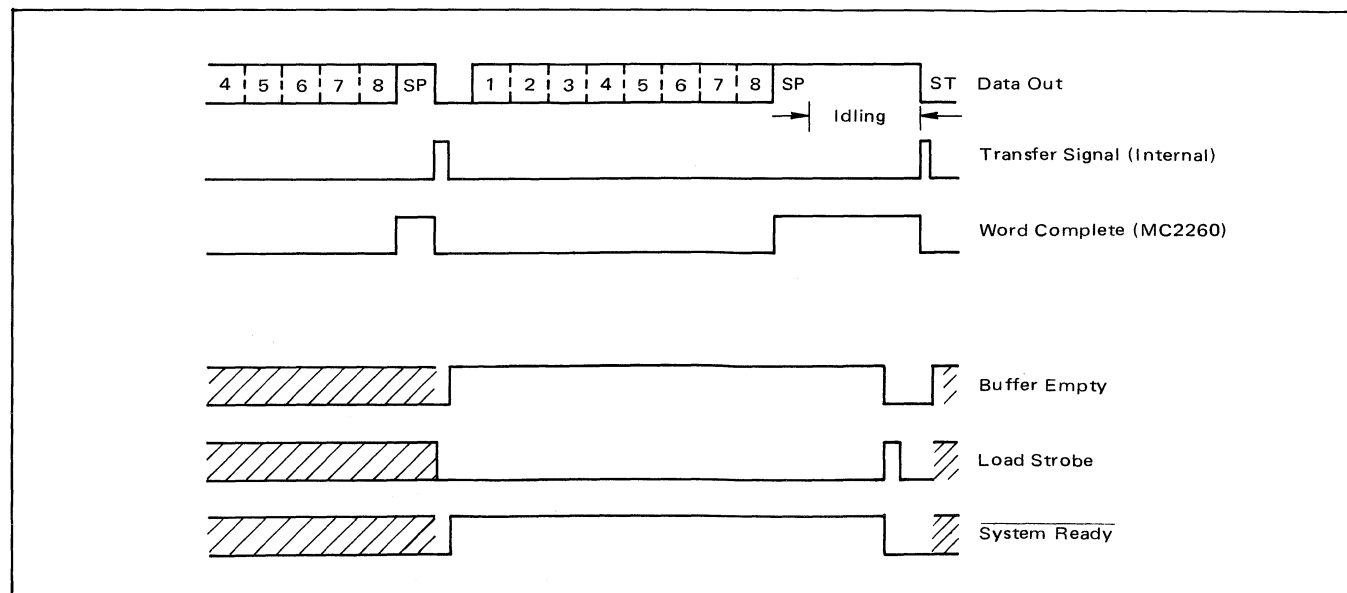

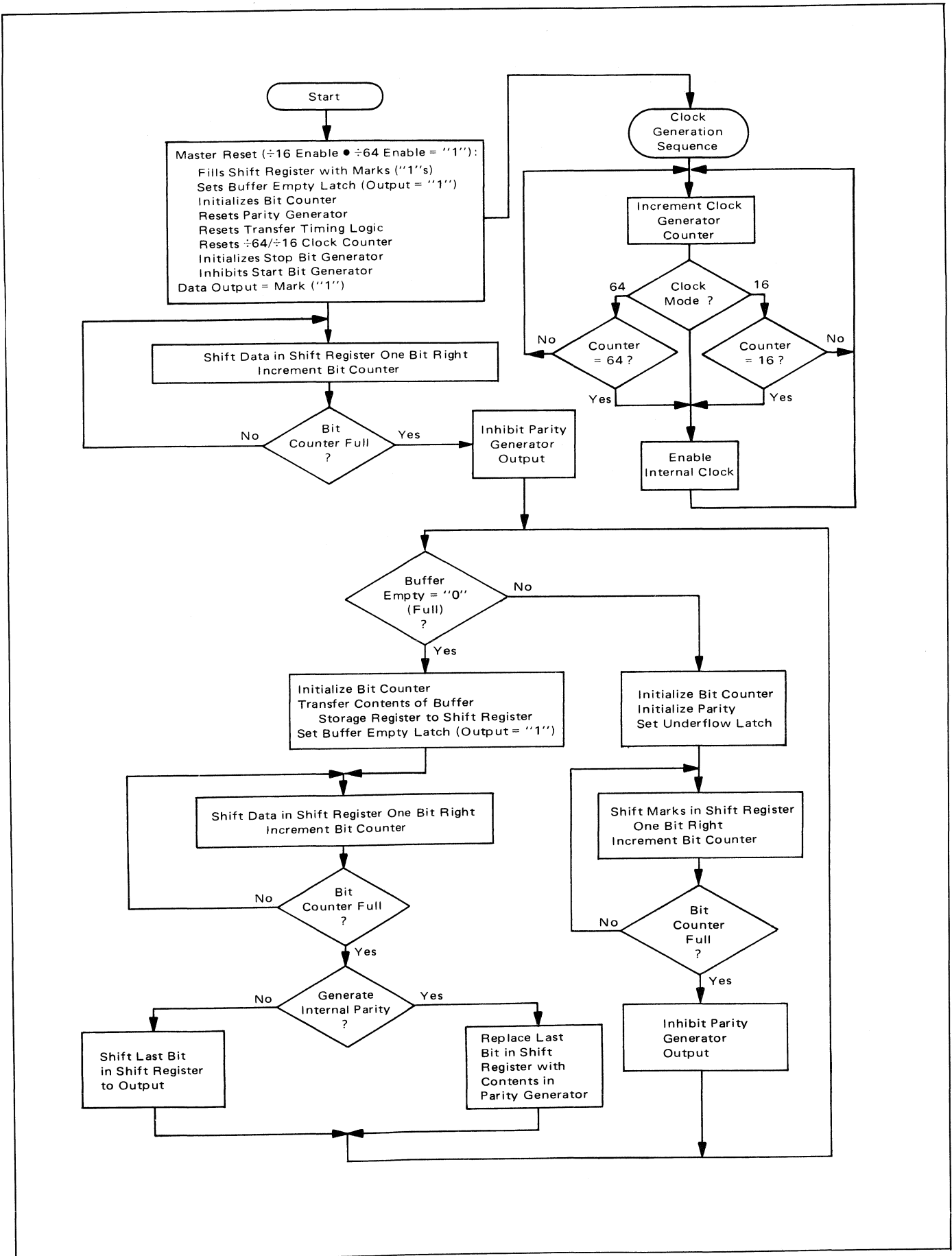**FIGURE 9 — Transmitter Idling During Transmission (Async Mode)**

```
                            ┌──────────┐                                    ╭──────────╮
                            │  Start   │                                    │  Clock   │
                            └────┬─────┘                                    │Generation│
                                 │                                          │ Sequence │
    ┌────────────────────────────────────────┐                             ╰────┬─────╯
    │ Master Reset (÷16 Enable ● ÷64 Enable = "1"):                              │
    │    Fills Shift Register with Marks ("1"'s)              ┌──────────────────────┐
    │    Sets Buffer Empty Latch (Output = "1")              │   Increment Clock     │
    │    Initializes Bit Counter                             │   Generator Counter   │
    │    Resets Parity Generator                             └───────────┬──────────┘
    │    Resets Transfer Timing Logic                                    │
    │    Resets ÷64/÷16 Clock Counter                            64  ╱ Clock ╲  16
    │    Initializes Stop Bit Generator                         ◄──┤  Mode ?  ├──►
    │    Inhibits Start Bit Generator                              ╲        ╱
    │ Data Output = Mark ("1")                                      ╲      ╱
    └────────────────────┬─────────────────────┘             ╱Counter╲      ╱Counter╲
                         │                              No ◄─┤ = 64 ? ├    ┤ = 16 ? ├─► No
    ┌────────────────────────────────────────┐               ╲      ╱        ╲      ╱
    │ Shift Data in Shift Register One Bit Right│              Yes               Yes
    │ Increment Bit Counter                     │               └────────┬────────┘
    └────────────────────┬─────────────────────┘                    ┌──────────┐
                         │                                           │  Enable  │
                  ╱   Bit    ╲     Yes      ┌──────────┐             │ Internal │
         No ◄────┤  Counter Full├──────────►│ Inhibit  │             │  Clock   │
                  ╲    ?      ╱             │ Parity   │             └──────────┘
                   ╲        ╱               │Generator │
                                            │ Output   │
                                            └────┬─────┘
                                                 │
                                          ╱   Buffer   ╲      No
                                         ┤  Empty = "0" ├──────────────────┐
                                         │    (Full)    │                  │
                                          ╲     ?      ╱                   │
                                               │ Yes                       │
              ┌───────────────────────────────┐          ┌────────────────────────┐
              │ Initialize Bit Counter         │          │ Initialize Bit Counter  │
              │ Transfer Contents of Buffer     │          │ Initialize Parity       │
              │   Storage Register to Shift Reg.│          │ Set Underflow Latch     │
              │ Set Buffer Empty Latch (Out="1")│          └───────────┬────────────┘
              └───────────────┬─────────────────┘                      │
                              │                          ┌──────────────────────────┐
              ┌───────────────────────────────┐          │ Shift Marks in Shift Reg. │
              │ Shift Data in Shift Register    │          │   One Bit Right           │
              │ One Bit Right                   │          │ Increment Bit Counter     │
              │ Increment Bit Counter           │          └───────────┬──────────────┘
              └───────────────┬─────────────────┘                      │
                       ╱   Bit    ╲                              ╱   Bit    ╲
              No ◄────┤  Counter Full├                  No ◄────┤  Counter  ├
                       ╲    ?      ╱                             ╲  Full ?  ╱
                            │ Yes                                     │ Yes
                  ╱ Generate  ╲  Yes                           ┌──────────────┐
          No ◄───┤  Internal   ├──►                            │   Inhibit    │
                 ╲  Parity ?  ╱                                │   Parity     │
           ┌──────────┐    ┌────────────┐                      │  Generator   │
           │Shift Last│    │Replace Last│                      │   Output     │
           │Bit in    │    │Bit in Shift│                      └──────────────┘
           │Shift Reg.│    │Register with│
           │to Output │    │Contents in  │
           └──────────┘    │Parity Gen.  │
                           └────────────┘
```

FIGURE 10 — MC2257 Terminal Transmitter Synchronous Operation Flow Diagram
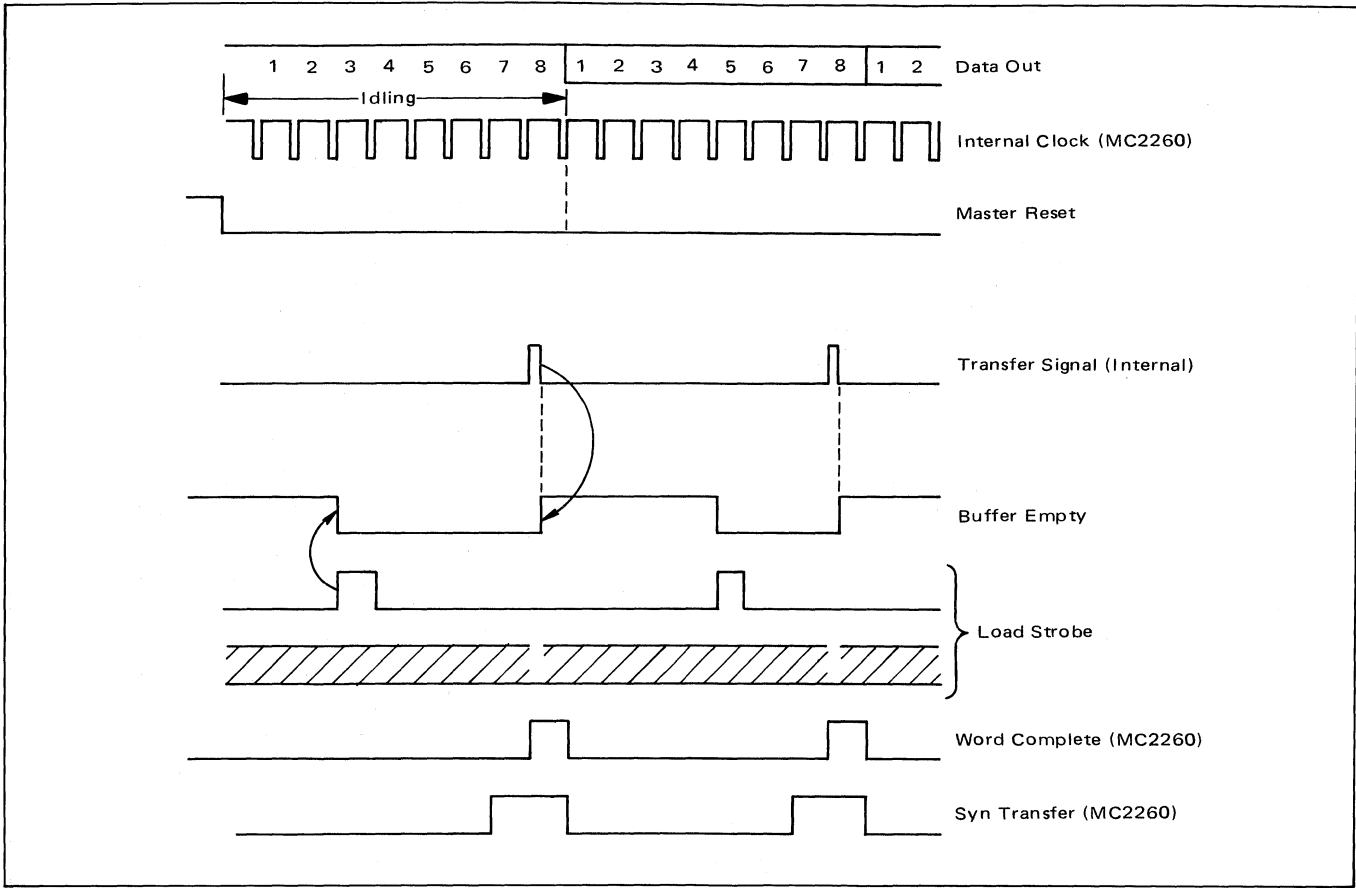
11

FIGURE 11 — Transmitter Synchronous Operation

register, and provide timing control to the sequence control logic for the insertion of parity (if internal parity is selected) into the last bit position of the character.

If data is not loaded into the buffer storage register, the Data Output is forced into an idling mode when the internal transfer signal is generated as shown in Figure 12. This idling time will occur in full character times. Therefore, N-character times of "marks" appear on the data output between transmission of characters (where N = 1,

2 . . . .). However, a sync character code can be transmitted in place of an idling character as a Fill Character. For example a sync character code may be loaded into the buffer which causes the Buffer Empty output to go "low". Then, the buffer register may be reloaded with a data character prior to the generation of the internal transfer signal which results in the data character being transmitted in place of the sync character. If a data character is not loaded into the buffer before the gener-
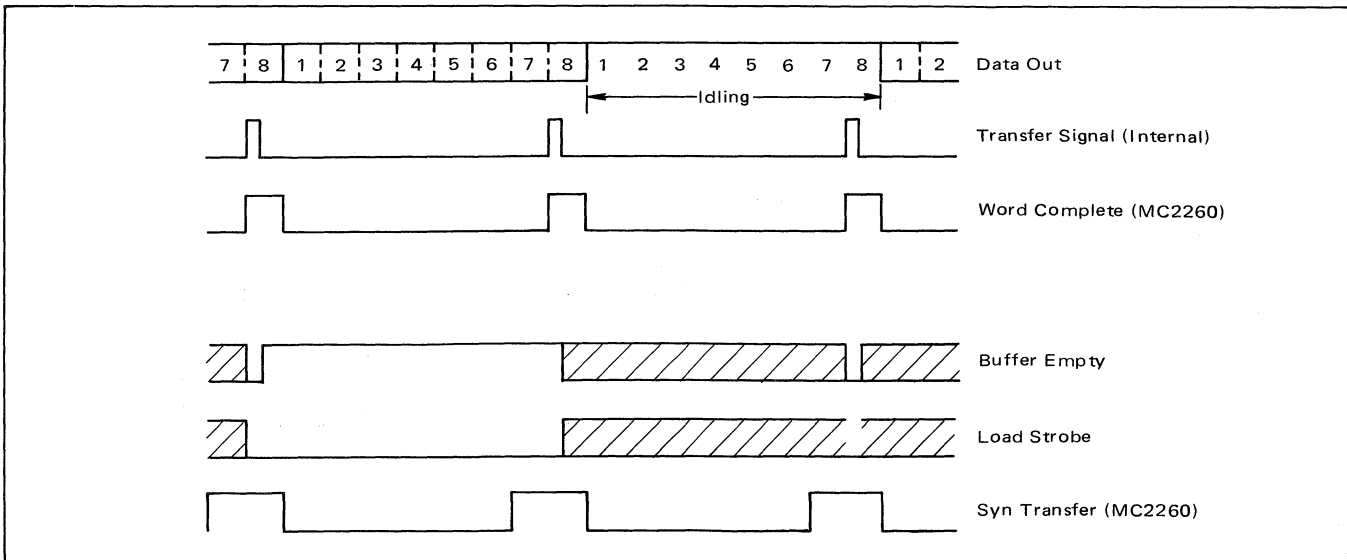
FIGURE 12 — Transmitter Idling During Transmission (Sync Mode)

12

ation of the internal transfer signal, the sync character code will be transmitted in place of the idling character. Also, the sync character provides a character synchronization check in the receiver during data transmission for precision systems.

The Syn Transfer output of the MC2260 is generated in the synchronous mode as shown in Figure 11. This output goes high during the last two bits of a synchronous character, and the internal transfer signal occurs at the approximate midpoint of the Syn Transfer signal. This output provides an indicator for loading a Sync character (Fill Character) one-bit time prior to the internal transfer time.

The Word Complete and Internal Clock outputs of the MC2260 are generated in the synchronous mode as shown in Figures 11 and 12. The Word Complete signal is generated during the last bit time of a data character or idling character.

TERMINAL RECEIVER (MC2259)

The terminal receiver can operate in either the asynchronous or synchronous mode. A general explanation of the operation of the receiver in these modes will be followed by the definitions of the input and output functions of the receiver. Then an explanation of both modes of operation with reference to timing diagrams will be discussed.

In the asynchronous mode, the normal state of the data line during the time when no character is being transmitted is the "mark" state. The format of the data in the asynchronous mode was shown in Figure 3 in the discussion of the transmitter. First, the receiver recognizes the start bit, then begins sampling each bit at its approximate midpoint. Each bit is serially shifted into a shift register and then automatically transferred to a buffer storage register when the character is complete.

In the Synchronous mode, the format of the data appears as a continuous bit stream with no interval between characters and no control bits (start and stop bit/s).

Therefore, synchronization must be accomplished by means of the characteristics of the data itself. Two degrees of synchronization must be performed: bit synchronization and character synchronization.

The technique of bit synchronization in the receiver uses each negative transition of the data. Each negative transition causes an incremental correction of the sampling position until it occurs at the midpoint of the data. The advantage of this technique is that data negative-transition times are averaged; therefore, signal-noise pulses or other data aberrations will have minimal effect on receiver bit synchronization.

Character synchronization is performed in the receiver in the following manner. A character sync code is sent as a preamble to the data message from the transmitter for establishing character synchronization. This sync character is shifted into the shift register where it is automatically gated to the output of the receiver. A sequence of comparisons between the received data and locally stored sync code are externally performed. Once coincidence is established, the synchronization sequence is complete, the external sync comparison logic is disabled and the incoming message is processed as data. Thereafter, an internal counter is used to maintain the character synchronization. If character synchronization is lost at any time, the "Syn" Detected input should be taken low and the process of establishing character synchronization repeated.

The receiver has several status indicators which are the result of a parity check, an absence of a stop bit, a lost character, and a transfer of data to the buffer register.

RECEIVER I/O

The inputs and outputs of the receiver are indicated on the block diagram of Figure 13 and the logic diagram of Figure 15. The functional flow diagram is shown in Figure 14. The definitions for each input and output are:

Data Strobe — The Buffer Storage latches are sampled whenever a high level is applied to the Data Strobe input. The Data Strobe can be held in the high state.
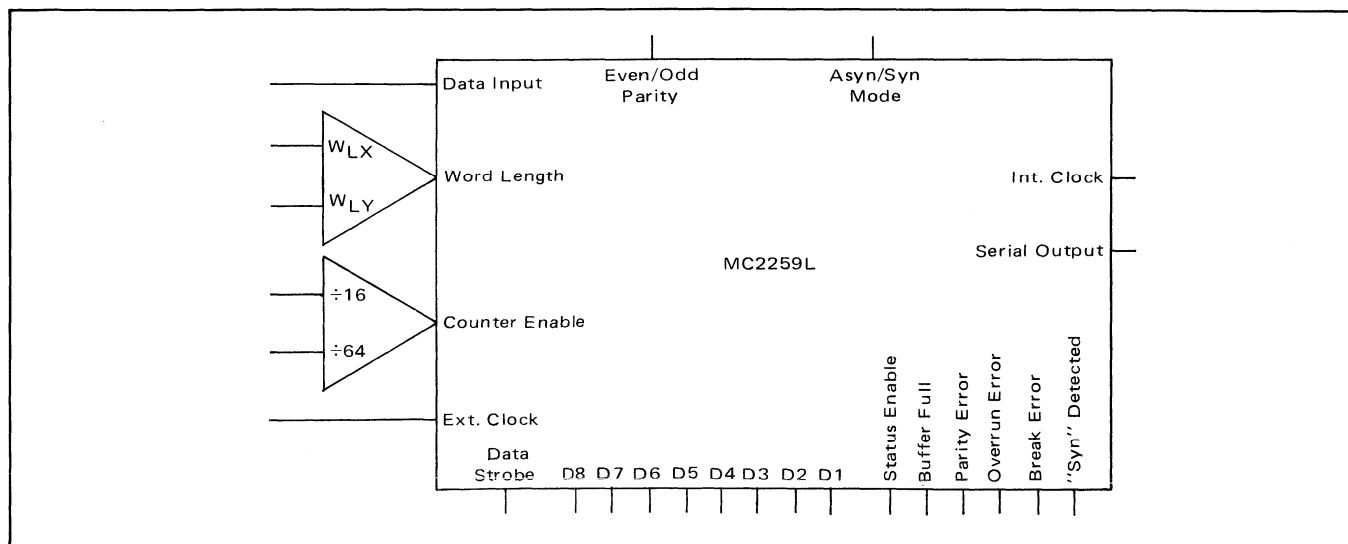

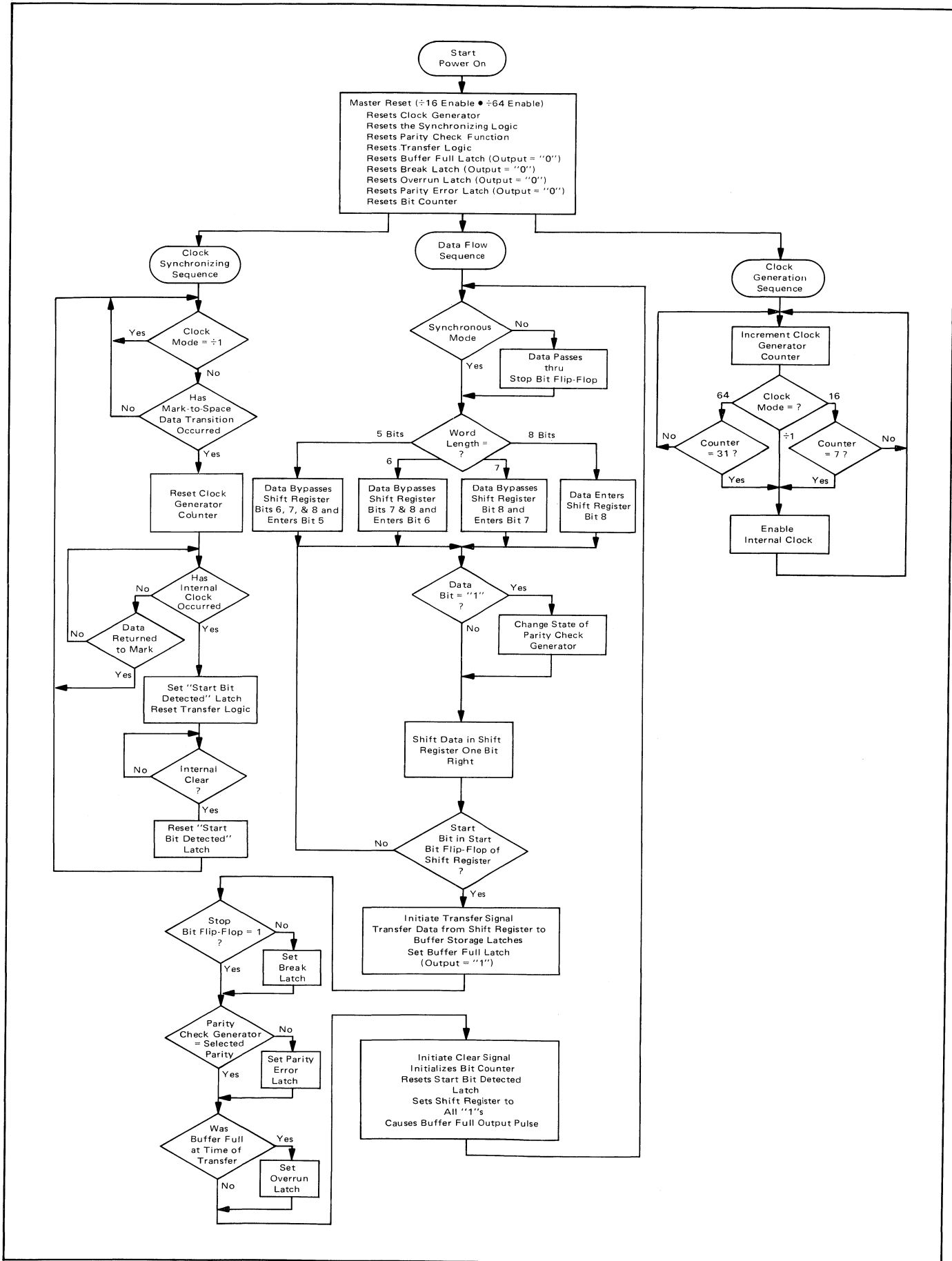FIGURE 13 – Terminal Receiver Block Diagram

Start
Power On

Master Reset (÷16 Enable ● ÷64 Enable)
Resets Clock Generator
Resets the Synchronizing Logic
Resets Parity Check Function
Resets Transfer Logic
Resets Buffer Full Latch (Output = "0")
Resets Break Latch (Output = "0")
Resets Overrun Latch (Output = "0")
Resets Parity Error Latch (Output = "0")
Resets Bit Counter

Clock Synchronizing Sequence

Data Flow Sequence

Clock Generation Sequence

Clock Mode = ÷1
Yes
No

Has Mark-to-Space Data Transition Occurred
No
Yes

Reset Clock Generator Counter

Synchronous Mode
No
Yes

Data Passes thru Stop Bit Flip-Flop

Increment Clock Generator Counter

64   Clock Mode = ?   16

Counter = 31 ?
No
Yes

÷1

Counter = 7 ?
No
Yes

Enable Internal Clock

Word Length = ?
5 Bits   8 Bits
6   7

Data Bypasses Shift Register Bits 6, 7, & 8 and Enters Bit 5

Data Bypasses Shift Register Bits 7 & 8 and Enters Bit 6

Data Bypasses Shift Register Bit 8 and Enters Bit 7

Data Enters Shift Register Bit 8

Has Internal Clock Occurred
No
Yes

Data Returned to Mark
No
Yes

Set "Start Bit Detected" Latch Reset Transfer Logic

Data Bit = "1" ?
Yes
No

Change State of Parity Check Generator

Internal Clear ?
No
Yes

Reset "Start Bit Detected" Latch

Shift Data in Shift Register One Bit Right

Start Bit in Start Bit Flip-Flop of Shift Register ?
No
Yes

Initiate Transfer Signal
Transfer Data from Shift Register to Buffer Storage Latches
Set Buffer Full Latch (Output = "1")

Stop Bit Flip-Flop = 1 ?
No
Yes

Set Break Latch

Parity Check Generator = Selected Parity
No
Yes

Set Parity Error Latch

Initiate Clear Signal
Initializes Bit Counter
Resets Start Bit Detected Latch
Sets Shift Register to All "1"s
Causes Buffer Full Output Pulse

Was Buffer Full at Time of Transfer
Yes
No

Set Overrun Latch

FIGURE 14 — MC2259 Terminal Receiver Asynchronous Operation Flow Diagram

14
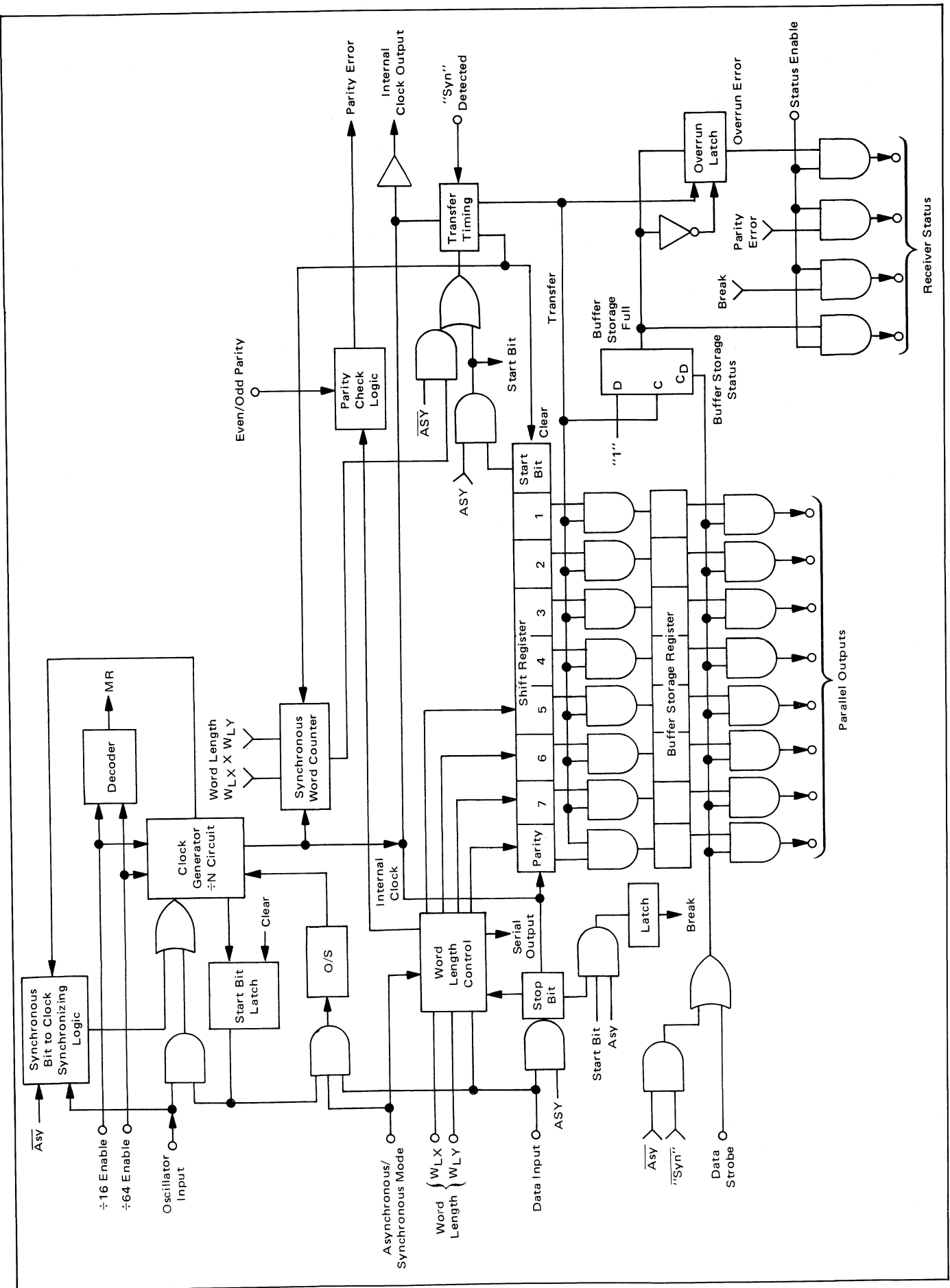
FIGURE 15 — MC2259 Terminal Receiver

External Clock Input — This is the oscillator input that controls the transmission rate of the receiver. In the ÷1 mode only, the negative transition of the external clock must occur at the approximate midpoint of the incoming data for bit synchronization. The external clock frequency is equal to the inverse of the product of the bit time (T) and the division mode of the receiver.

÷16 and ÷64 Counter Enables — These two inputs provide a means of producing the internal clock from an oscillator that is either 16 or 64 times the bit rate. Provision is also made to bring the already synchronized clock from a source such as a modem into the Terminal Receiver to act as the internal clock. Available options are shown in the following table.

÷16	÷64	Oscillator Frequency at the External Clock Input
0	0	= Bit Rate (÷1)
1	0	= 16 x Bit Rate
0	1	= 64 x Bit Rate
1	1	Master Reset*

*A typical design of the external system is such that one of the divider enables is selected for the applicable external clock frequency. The other enable input then becomes a Master Reset for the Terminal Receiver.

Word Length Selector — Two input lines (W_{LX}, W_{LY}) are provided to define the character bit length. A character will always appear at the output in a right justified bit position for the selected word lengths. The following table shows the character length for each input combination.

W_{LX}	W_{LY}	Word Length (Including parity, if applicable)
1	1	8 bits
0	1	7 bits
1	0	6 bits
0	0	5 bits

A high level is defined as a positive logic "1". These inputs may be changed only during an idling condition or master reset.

Data Input — The serial data from the modem or other source is entered into the Terminal Receiver by means of this input. Data is not inverted within the receiver and appears at the output in the same sense as it enters.

Even/Odd Parity — A high level on the Even/Odd Parity input causes a check for an even number of high-level data bits, including the parity bit. A low level checks for odd parity in a similar manner. There is no provision to inhibit the Parity Check logic for "no parity" data transmission. This input may be changed at any time except during the internal transfer time.

Asynchronous/Synchronous Mode — A high level on the Asynchronous/Synchronous Mode input enables the device for operation in the asynchronous mode using control bits (START and STOP). The START bit is used to indicate the presence of a character and for synchronization of the internal clock with the character. The presence of a STOP bit verifies character synchronization.

A low level on this input enables the device for synchronous operation and disables all asynchronous logic. In the ÷16 or ÷64 modes, a transition monitor samples each "mark-to-Space" transition of the data, compares the ÷16/÷64 clock counter state with the preferred coincidence state, and incrementally adjusts in one-half clock-steps toward correct bit synchronization. In the ÷1 mode, bit synchronization must be accomplished externally. Character synchronization is handled externally by detecting a series of sync characters.

Internal Clock Output — The internal clock that has been synchronized with the data is available for external use by means of this output.

Serial Output — The data being shifted into the shift register is simultaneously available at the Serial Output. This provides a means for externally accumulating longitudinal parity.

"Syn" Detected (Synchronous Mode only) — A low level applied to this line holds the Buffer Storage Register latches open so that data ripples across the outputs to permit external detection of sync codes on the receiver outputs. A transition to a high level indicates to the receiver that the external logic has determined character sync. A high level on this input enables the system to operate in the synchronous mode by cycling in synchronization with each character.

Receiver Status Outputs — Status information is provided by means of four open-drain outputs. These outputs are enabled by the Status Enable input and can be used in bussing configurations. The functions of these Status outputs are:

1. Break (Asynchronous Mode only) — The absence of a STOP bit following the character causes a Break signal to be stored in the Receiver Status Register for the character time.

2. Overrun — This output provides an indication that two or more characters have been transferred into the Buffer Storage Register latches in succession without an intervening sampling of the buffer contents by use of the Data Strobe. This means that at least one character has been lost. Use of the Data Strobe removes this indicator after the transfer of the next character into the Buffer Storage Register.

3. Parity Error — Incorrect parity for a particular character causes an error signal (high level) to be generated and made available at the Parity Error output for the period that the character is present in the Buffer Storage Register.

4. Buffer Full — This output shows that a character is in the Buffer Storage latches and has not been sampled at the eight data outputs by using the Data Strobe input. The Data Strobe signal automatically resets the Buffer Full outputs. If the Data Strobe input is maintained in the high state, the Buffer Full output will appear as a pulse when a character is transferred from the shift register to the buffer register.

Status Enable — The latches of the Receiver Status Register are sampled whenever a high level is applied to the Status Enable line. The Status Enable may be maintained in the high state. This input may be changed at any time.

Data Outputs — Data is transferred to the eight parallel open-drain outputs from the Buffer Storage Register latches with a high on the Data Strobe input. Data appears in a right justified position independent of the character length.

ASYNCHRONOUS OPERATION

Refer to the functional block diagram (Figure 15) and the flow chart of Figure 14 as an aid to understanding the operating sequence.

A function of the receiver is to respond to and synchronize with incoming data. A master reset of the receiver is required to initialize the internal circuitry to ensure correct system operation. During the master reset time and between transmission of characters the Serial Data input must be in the idling mode or "Mark" condition to achieve character synchronization. The initial change in the state of this line after release of master reset will occur upon receipt of the start bit from the transmitting source. First, the "mark-to-space" transition of the start bit causes the internal clock generator to be initialized for synchronization of the internal clock with the data. Then, the Serial Data input is continuously monitored until the internal clock signal is generated at the approximate midpoint of a valid start bit as shown in Figure 16 for the divide by 16 mode.

The characteristics of the Internal Clock generated for the full character time for the ÷16 and ÷64 mode are shown in Figure 17. (The Internal Clock output is not generated during master reset, idling or second stop bit time except for the ÷1 mode as shown in this figure). The tolerance requirements of the external clock that generates the internal clock depends upon the minimum duration of a bit interval with respect to its midpoint, and the number of bits per character (accumulative error); minimum duration as used here means the nominal transmitted signal less any uncertainty caused by phase jitter, distortion, etc., as shown in Figure 18. Additional distortion can be caused by the fact that the start bit transition may occur up to one external clock period prior to its detection. This means that the actual center of the data bit interval may be skewed as much as one external clock period to the right of the sampling pulse (Internal Clock) as shown in Figure 19. For the ÷16 mode, this skew amounts to 1/16 of a data bit interval, and for the ÷64 mode, it is 1/64 of a data bit interval. Therefore, from these considerations, the required tolerance (Δf) can be determined from the following equation:

$$\Delta f = \frac{[\pm(X)\%] - Y\%}{Z}$$

where X = 1/2 of the minimum duration of a bit interval centered around the nominal midpoint

Y = Maximum possible shew between external clock and start bit transition
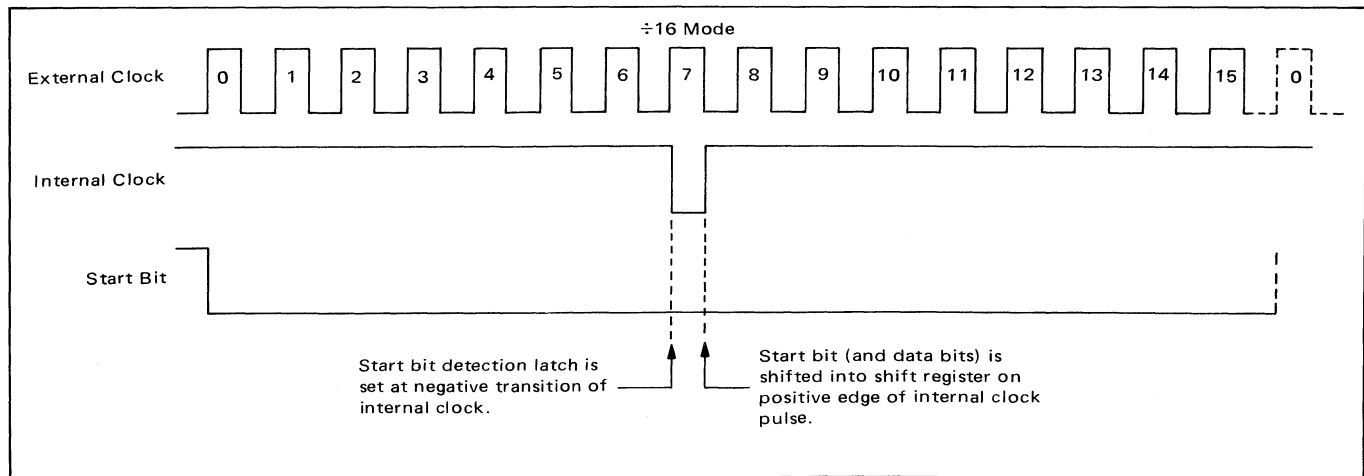
Z = Number of bits/character

FIGURE 16 — False Start Bit Deletion in Receiver

Once a valid start bit has been detected, bit and character synchronization have been obtained for the full character. However, if the data input returns to the mark state (as in the case of noise) during the monitoring period, the bit is ignored and the receiver resumes looking for the mark to space transition of a valid start bit. This process is referred to as False Start Bit Deletion and assures the presence of a valid start bit. The receiver repeats this process of bit character synchronization for each character.

The number of bits/character does not include the second stop bit because the receiver does not sample this stop bit. For example, a typical system with a minimum duration of 50% (X = 25%) operating in the ÷16 mode (Y = 6.2%) with 10 bits/character, the required tolerance of the external clock (Δf) is Δf = +1.88 to –3.12%. The frequency tolerance is not symmetrial because the skew (Y) does not center about the midpoint of the nominal data interval.
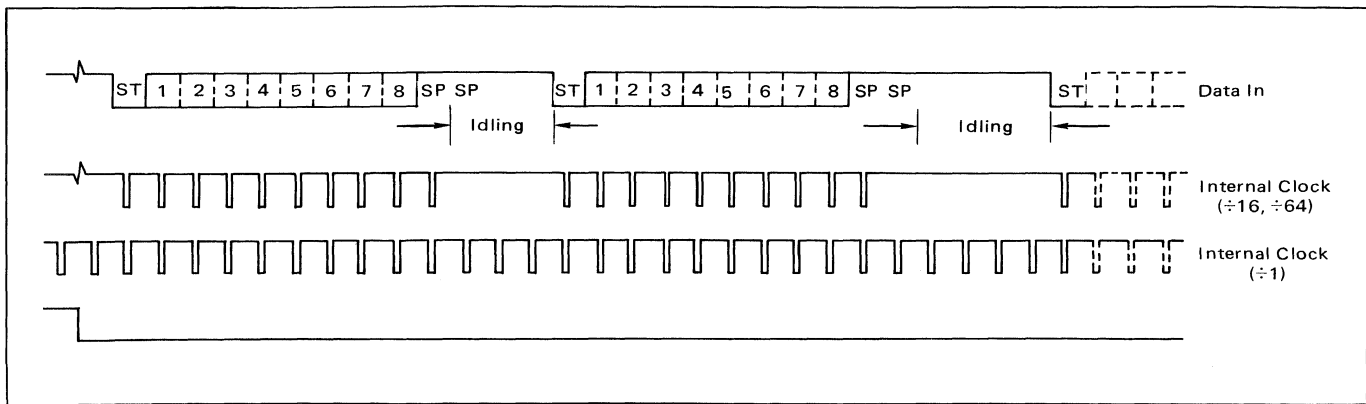
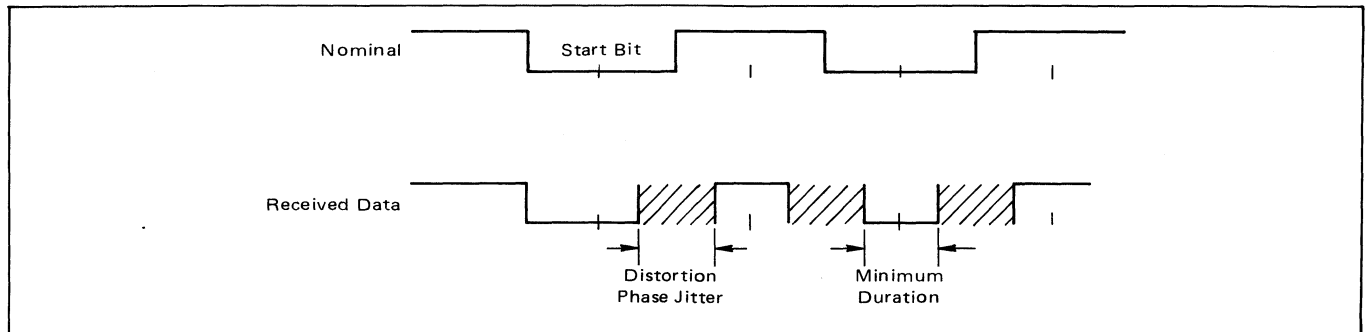**FIGURE 17 — Receiver Internal Clock (Asyn Mode)**

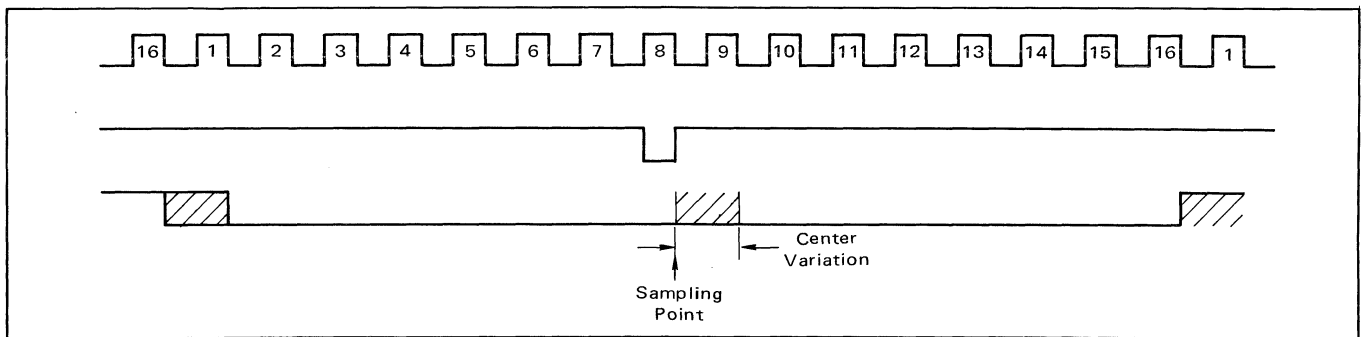**FIGURE 18 — Data Distortion**

FIGURE 19 — Receiver Sampling Technique (Asyn Mode)

After the start bit is detected and the synchronization is accomplished, the character (including start and stop bits) is serially shifted through the shift register until the start bit appears in the start bit flip-flop (the last stage of the shift register which has no external connection). The complete character is now stored in the shift register and the receiver automatically generates a transfer signal to load the character in the buffer storage register. The generation of the transfer signal is shown in Figure 20. Also, the transfer signal clocks the four status output flip-flops: Break, Overrun, Parity Error, and Buffer Full.

The absence of the first stop bit of a character will result in an error output (Break) to occur when the internal transfer is generated as shown in Figure 21. If a Break Error occurs, the next correct character or a master reset will reset the Break Error output. The design of the receiver is such that the absence of the first stop bit does not cause the receiver to lose bit and character synchronization.

As the character shifts through the shift register, parity for the character is accumulated. The resulting parity (Figure 21) is compared with correct parity (odd or even) and, in the case of error, Parity Error will be stored in the receiver status register when the internal transfer signal is generated. The receiver only checks for parity and does not strip the parity bit from the character. This permits the parity bit to be retained throughout the system without generating new parity bits. The parity checking logic cannot be inhibited in the receiver and, therefore, the Parity Error output should be ingored if parity is not utilized in transmission. If a parity error occurs, the next correct character or master reset will reset the Parity Error output.
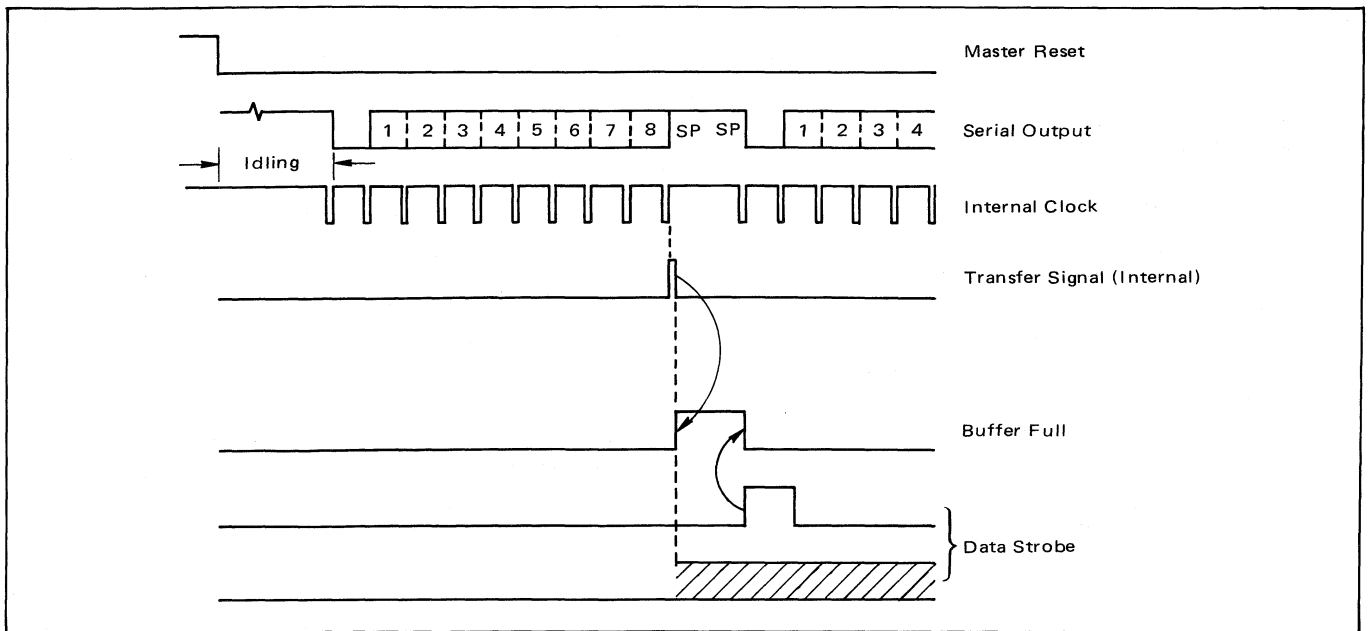
18

FIGURE 20 — Receiver Asynchronous Mode
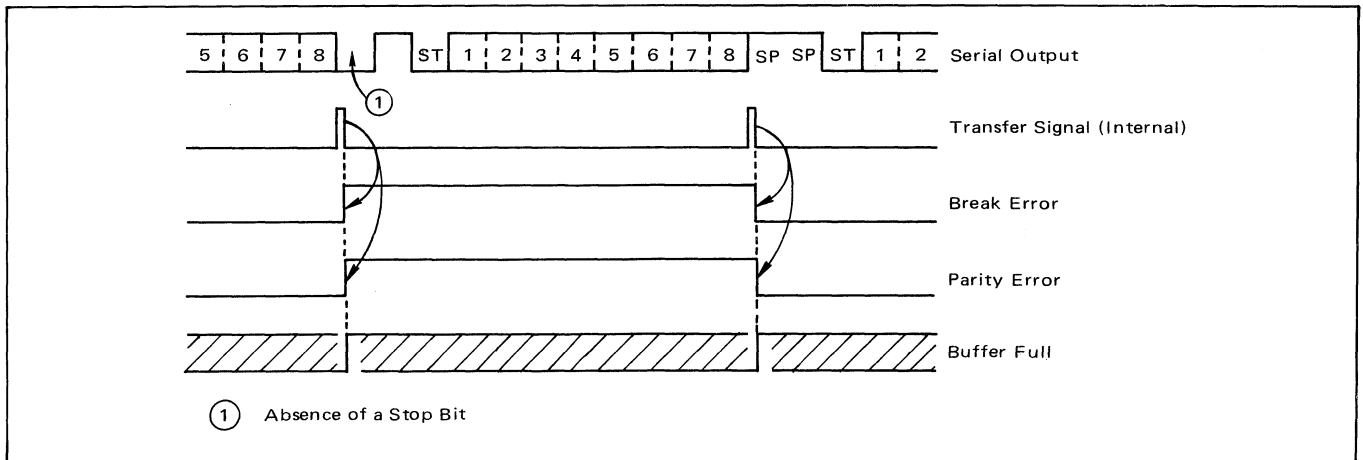

① Absence of a Stop Bit

FIGURE 21 — Receiver Break and Parity Error (Asyn Mode)

When the character is transferred to the buffer storage register a Buffer Full signal is generated by the internal transfer signal as shown in Figure 20. The positive edge of the Data Strobe resets the Buffer Full output while the positive level of the Data Strobe enables the Data Outputs; a logic "0" on the Data Strobe allows the Data Outputs to float. If a Data Strobe pulse does not occur during a character time, the Buffer Full signal is not reset and the internal transfer signal causes the overrun condition to occur as shown in Figure 22. Therefore, the Overrun Error output indicates that a Data Strobe did not occur during a complete character time and at least one
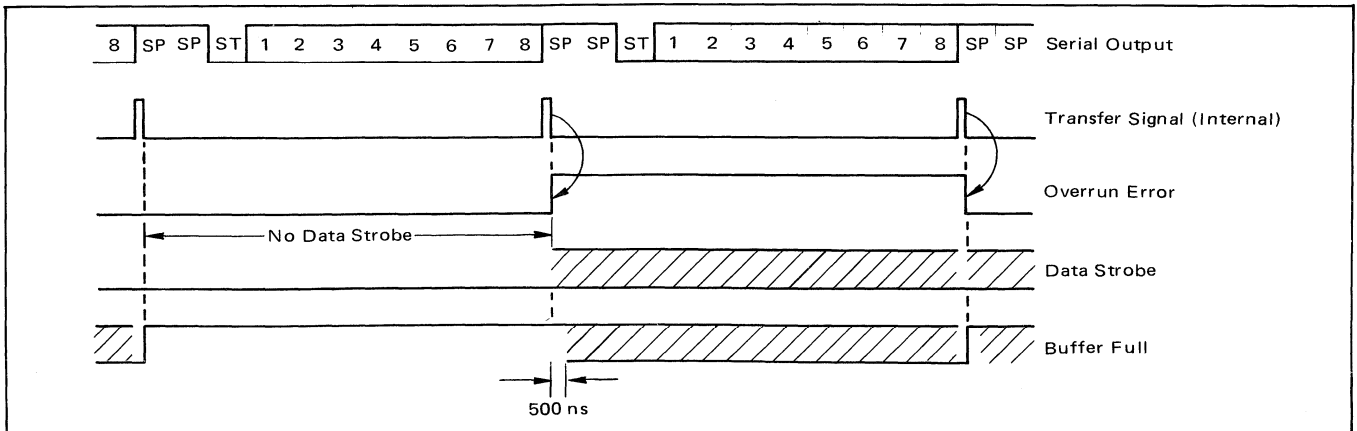

FIGURE 22 — Receiver Overrun Error (Asyn Mode)

character is lost. After an overrun condition occurs the application of the Data Strobe will reset the Buffer Full and cause the Overrun output to reset when the internal transfer signal is generated as shown in Figure 22.

During the above operation, the Serial Output is decoded from the first flip-flop (stop bit flip-flop) of the shift register in the asynchronous mode. The data on the serial output is delayed from the data arriving at the receiver dependent on the generation of the internal clock as shown in Figure 23. Then the detection of the start bit in the last position of the right justified shift register causes an internal clear of the shift register which resets the stop bit flip-flop. The reset of the stop bit flip-flop occurs after the examination of the stop bit flip-flop for a break condition. Therefore, the absence of a stop bit results in the Serial Output appearing to have a valid stop bit due to the reset action, but will result in a Break Error occurring.

The receiver treats the second stop bit as though it were an idling bit. This capability enables the receiver to receive a format which consists of one stop bit and a partial stop bit. An example of this format is a teletypewriter which transmits 1.42 stop bits.

Bit and character synchronization must be performed by examining the characteristics of the data in order to receive a valid message. However, bit synchronization has to be performed before character synchronization can be established. Therefore, the bit synchronization process will be discussed first.

The technique of bit synchronization provided in the terminal receiver utilizes each "Mark-to-Space" (negative) transition of the data in the ÷16 and ÷64 modes. Each negative transition of the data causes an incremental correction of the internal clock to the data bit. This incremental correction is equal to half an external clock period which is equal to 1/32 (÷16 mode) or 1/128 (÷64 mode) of a bit time for a 50% duty cycle external clock. The process of incrementing the clock with respect to the received data continues with each "Mark-to-Space" transition in order to generate the internal clock pulse at the approximate midpoint of the data, i.e., the data is sampled at the positive transition of the internal clock pulse. The advantage of this technique is that data negative transition times are averaged; therefore signal noise pulses or data aberrations will not cause the receiver to completely
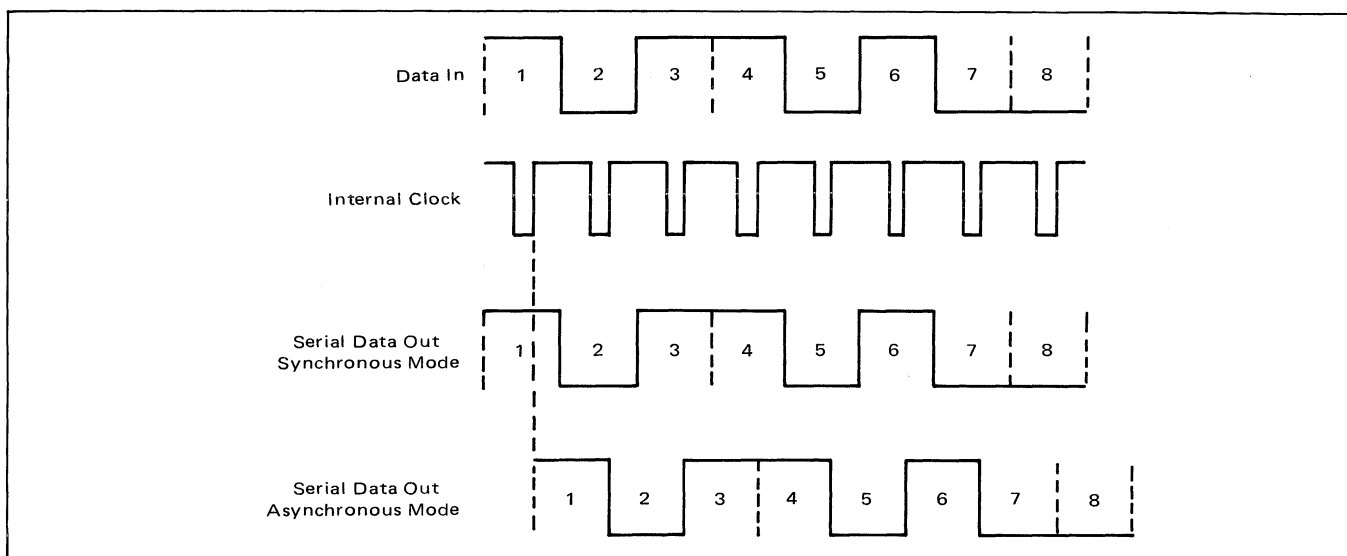

FIGURE 23 — Receiver Serial Data Out

SYNCHRONOUS OPERATION

The flow diagram shown in Figure 24 should be used as an aid in understanding synchronous operation of the receiver.

Synchronous data, as mentioned earlier, appears as a continuous bit stream of data bits without control bits (start and stop bits). Also, idling between characters due to non-transmission of data is in multiples of character lengths. (The terminal transmitter (MC2257, MC2260) automatically generates a full idling character during non-transmission of data as was shown in Figure 12.) The explanation of the synchronous operation of the receiver assumes that there is no degradation of the received data, and that the external clock frequency is 100% accurate.

lose bit synchronization and thereby in turn lose character synchronization.

Character synchronization is performed external to the terminal receiver by means of a sequence of comparisons between the received data and the reference sync code. With the "Syn" Detect input "low" and the receiver in the synchronous mode the buffer storage register is "transparent" so that data can be monitored as it ripples through the shift register. Once character synchronization has been performed externally, the "Syn" Detected input is returned to a "high" state which returns the buffer storage register to its normal operation. Then, the next character which could be a sync code for verification of synchronization is automatically transferred to the buffer
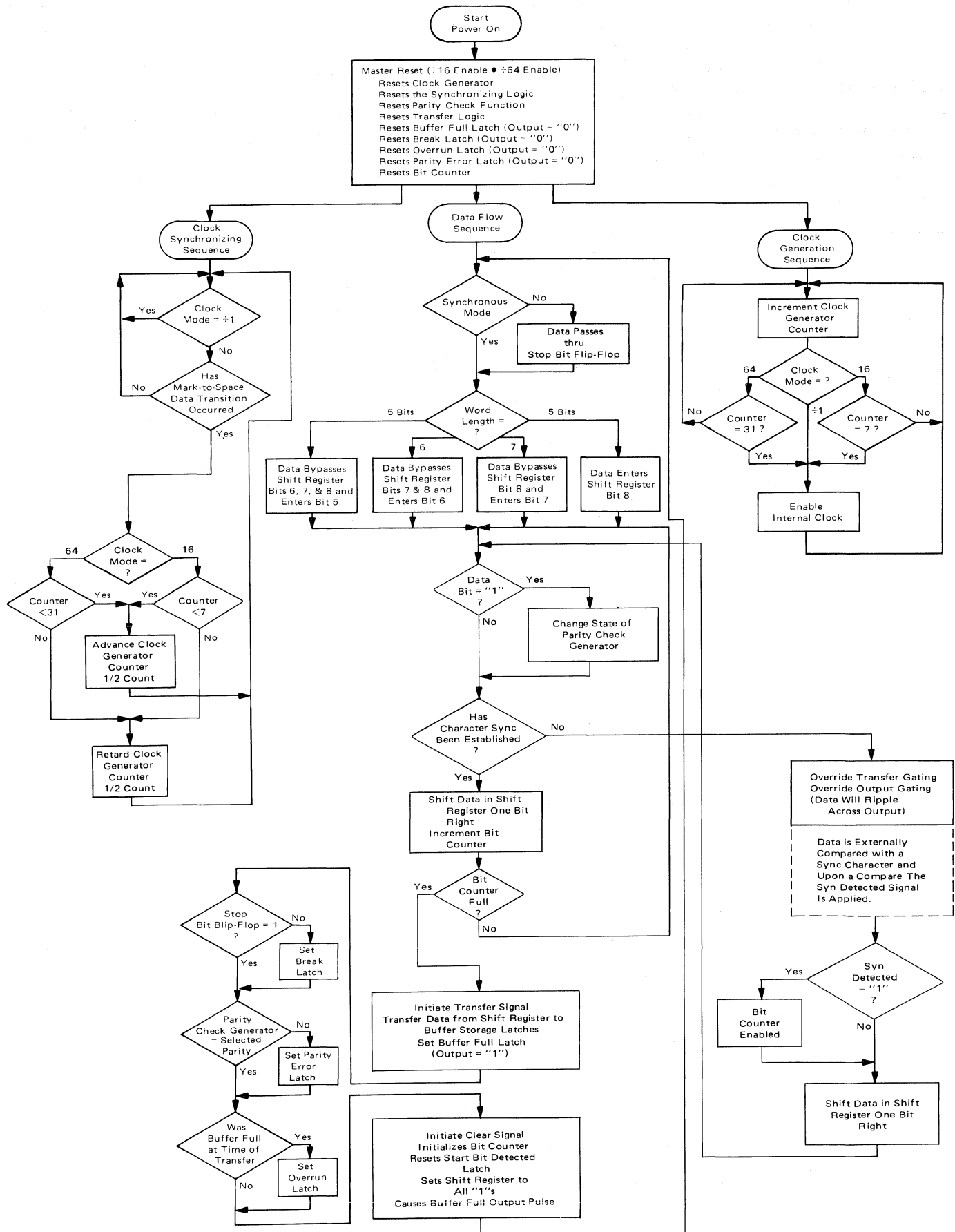
Start
Power On

Master Reset (÷16 Enable ● ÷64 Enable)
Resets Clock Generator
Resets the Synchronizing Logic
Resets Parity Check Function
Resets Transfer Logic
Resets Buffer Full Latch (Output = "0")
Resets Break Latch (Output = "0")
Resets Overrun Latch (Output = "0")
Resets Parity Error Latch (Output = "0")
Resets Bit Counter

Clock Synchronizing Sequence

Data Flow Sequence

Clock Generation Sequence

Clock Mode = ÷1 — Yes

No

Has Mark-to-Space Data Transition Occurred — No / Yes

Synchronous Mode — No → Data Passes thru Stop Bit Flip-Flop

Yes

Increment Clock Generator Counter

64 / Clock Mode = ? / 16 / ÷1
Counter = 31 ? — No / Yes
Counter = 7 ? — No / Yes

Enable Internal Clock

Word Length = ? — 5 Bits / 5 Bits / 6 / 7

64 / Clock Mode = ? / 16
Counter <31 — Yes / Yes — Counter <7
No / No

Advance Clock Generator Counter 1/2 Count

Retard Clock Generator Counter 1/2 Count

Data Bypasses Shift Register Bits 6, 7, & 8 and Enters Bit 5

Data Bypasses Shift Register Bits 7 & 8 and Enters Bit 6

Data Bypasses Shift Register Bit 8 and Enters Bit 7

Data Enters Shift Register Bit 8

Data Bit = "1" ? — Yes → Change State of Parity Check Generator
No

Has Character Sync Been Established ? — No
Yes

Shift Data in Shift Register One Bit Right Increment Bit Counter

Override Transfer Gating Override Output Gating (Data Will Ripple Across Output)

Data is Externally Compared with a Sync Character and Upon a Compare The Syn Detected Signal Is Applied.

Stop Bit Blip-Flop = 1 ? — No → Set Break Latch
Yes

Parity Check Generator = Selected Parity — No → Set Parity Error Latch
Yes

Bit Counter Full ? — Yes / No

Syn Detected = "1" ? — Yes → Bit Counter Enabled
No

Was Buffer Full at Time of Transfer — Yes → Set Overrun Latch
No

Initiate Transfer Signal Transfer Data from Shift Register to Buffer Storage Latches Set Buffer Full Latch (Output = "1")

Shift Data in Shift Register One Bit Right

Initiate Clear Signal Initializes Bit Counter Resets Start Bit Detected Latch Sets Shift Register to All "1"s Causes Buffer Full Output Pulse

FIGURE 24 – MC2259 Terminal Receiver Synchronous Operation Flow Diagram

21

storage register when complete. If character synchronization is lost at any time, the "Syn" Detected should be taken "low" and the synchronization process repeated. The outputs of the status register are inhibited when the "Syn" Detected input is "low". One example of the logic for the external character synchronization is shown in Figure 25. A one-shot is required to allow the data outputs to settle. Once the synchronization sequence is complete, the external sync comparison logic is disabled and the incoming data message is processed as data.

In the asynchronous mode, data was serially shifted through the stop bit flip-flop and character synchronization was maintained by the detection of the start bit. In the synchronous mode, data is still serially shifted but bypasses the stop-bit flip-flop and a bit counter is used to maintain character synchronization. When the final data bit is shifted into the shift register, the internal bit counter generates an internal transfer signal as shown in Figure 26. The internal transfer signal transfers the data from the shift register to the buffer register, and at the same time
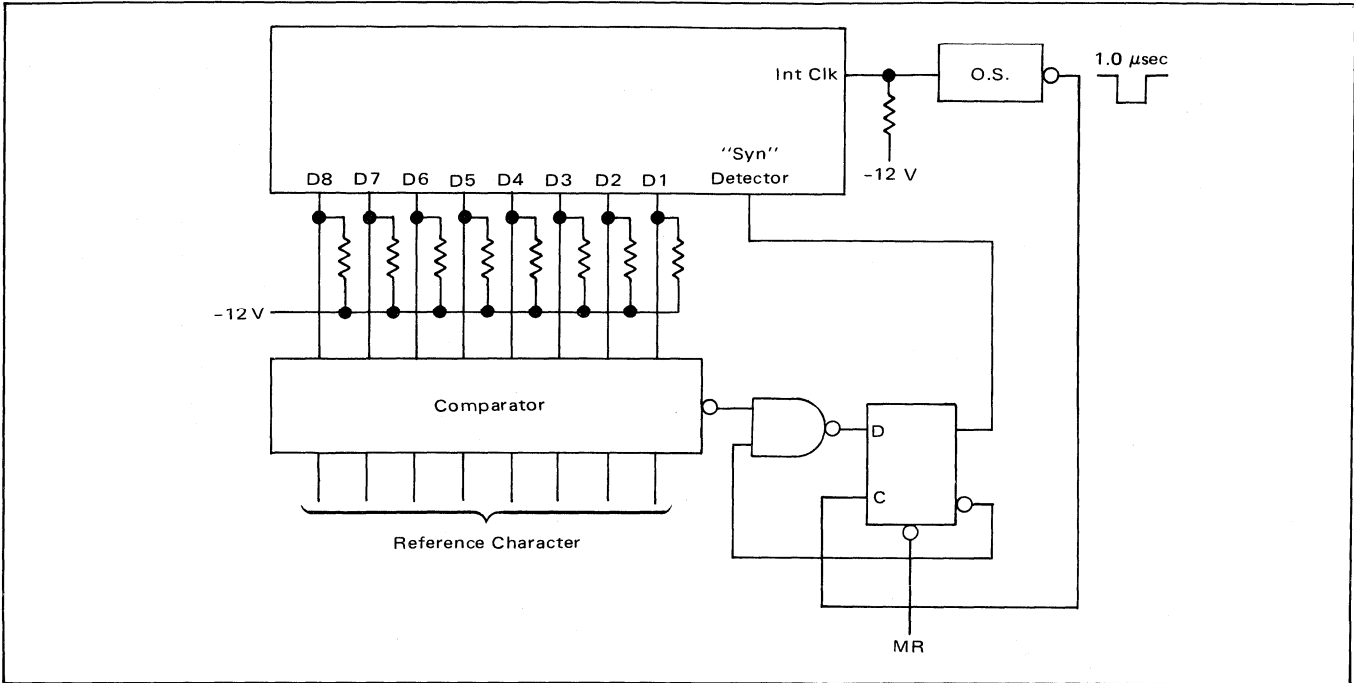
FIGURE 25 — External Character Synchronization
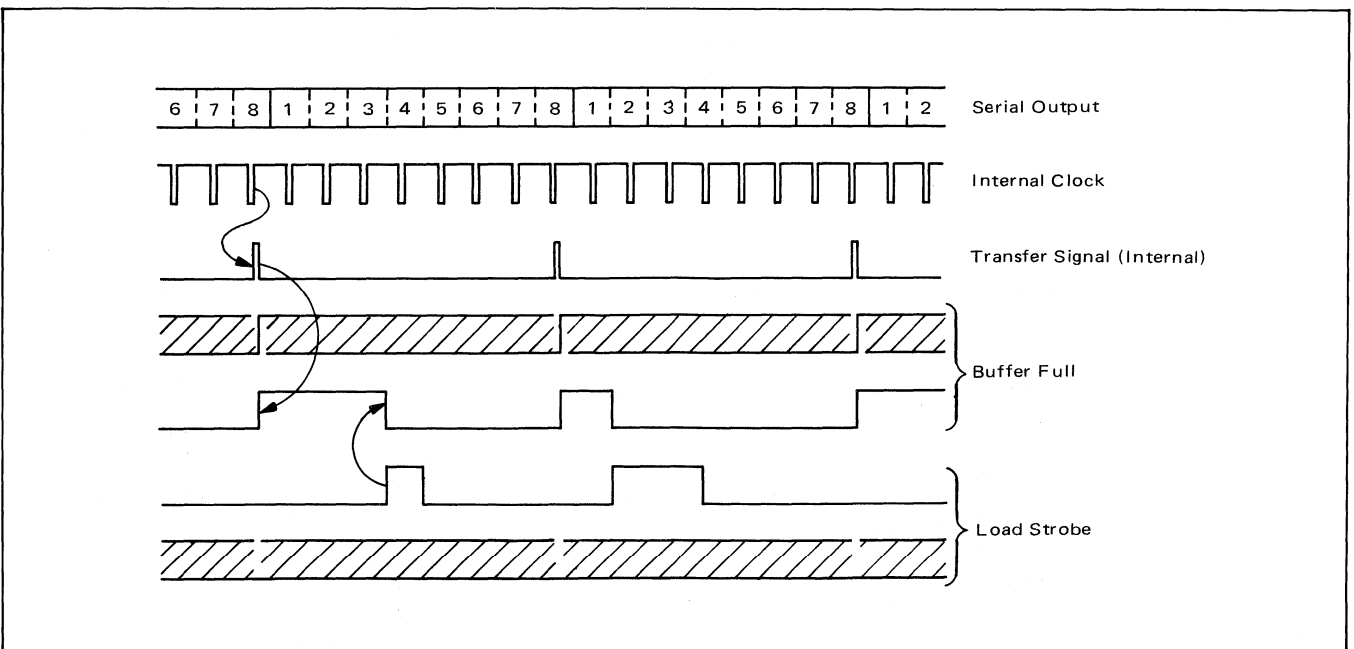
FIGURE 26 — Receiver Synchronous Mode

causes the Buffer Full output to go "high". Also, the internal transfer signal generates a Parity Error and Overrun Error if they exist as shown in Figure 27. The duration and reset of the Overrun and Parity Errors outputs are similar to the asynchronous mode characteristics. Since there are no stop bits in the synchronous mode, the Break Error output will remain "low".

The Serial Output in the synchronous mode is the data entering the receiver gated to the serial output. Therefore, the data on the Serial Output is identical to the incoming data bits but delayed in time by several gate delays.

protected as is commonly done in PMOS devices. Therefore, a positive logic "one" can be achieved by either holding the input "high" or by allowing it to "float".

All outputs require a pulldown resistor of approximately 6.8 k ohms to -12.0 V (V_{GG}) to be capable of interfacing with one TTL load as shown in Figure 29a. In the case where the Buffer Empty is tied to the System Ready the pulldown resistor can vary from 6.8 k to about 50 k ohms. This resistor value range applies for any interfacing of a PMOS output to a PMOS input on the transmitter and receiver. The outputs and inputs can be made
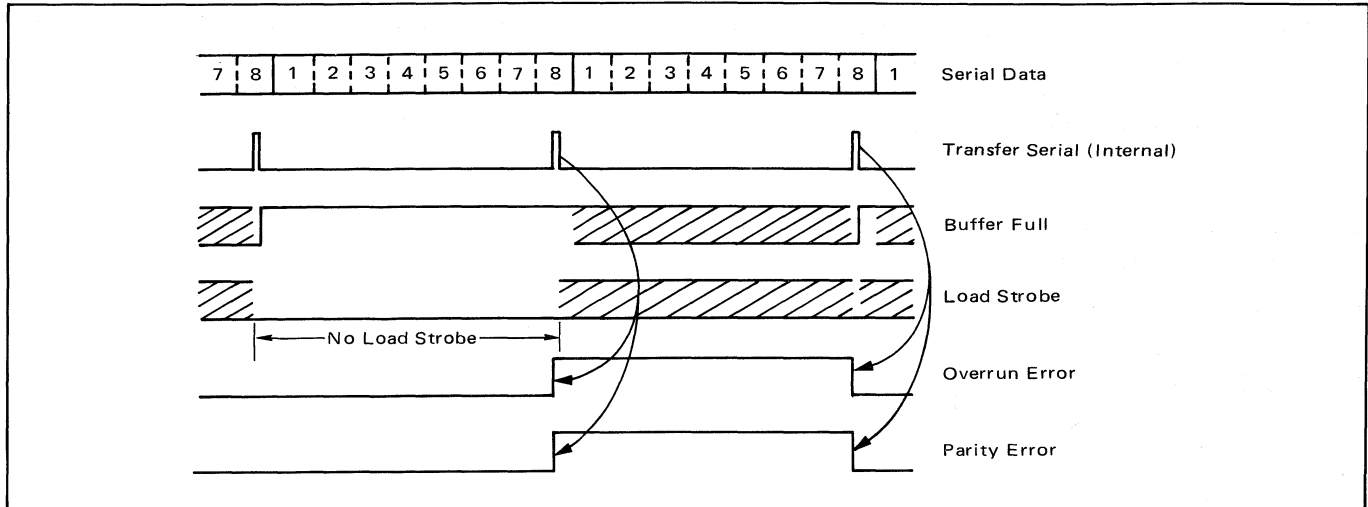
FIGURE 27 — Receiver Overrun and Parity Error (Syn Mode)

DEVICE INPUT AND OUTPUT CHARACTERISTICS

The inputs of the terminal transmitter and receiver are internally biased "high" through an equivalent resistance of 20 k ohms to V_{SS} which provides for higher noise immunity when driven by TTL and also simulates a TTL input as shown in Figure 28. Also, the inputs are diode
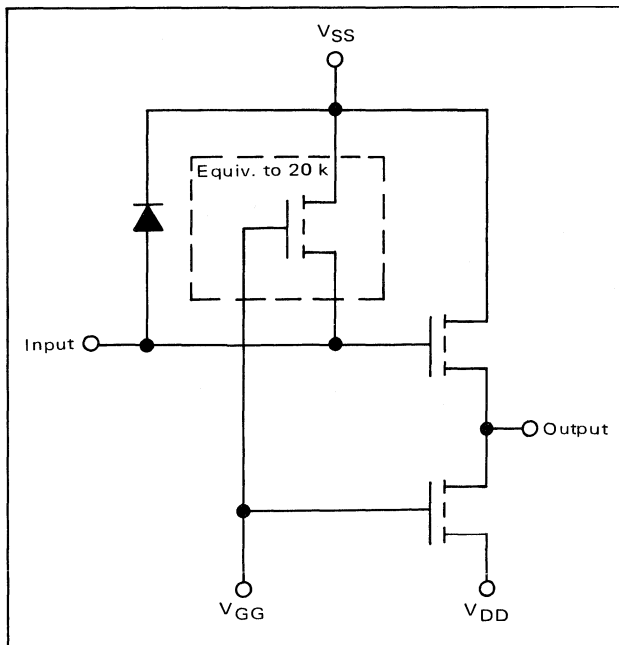

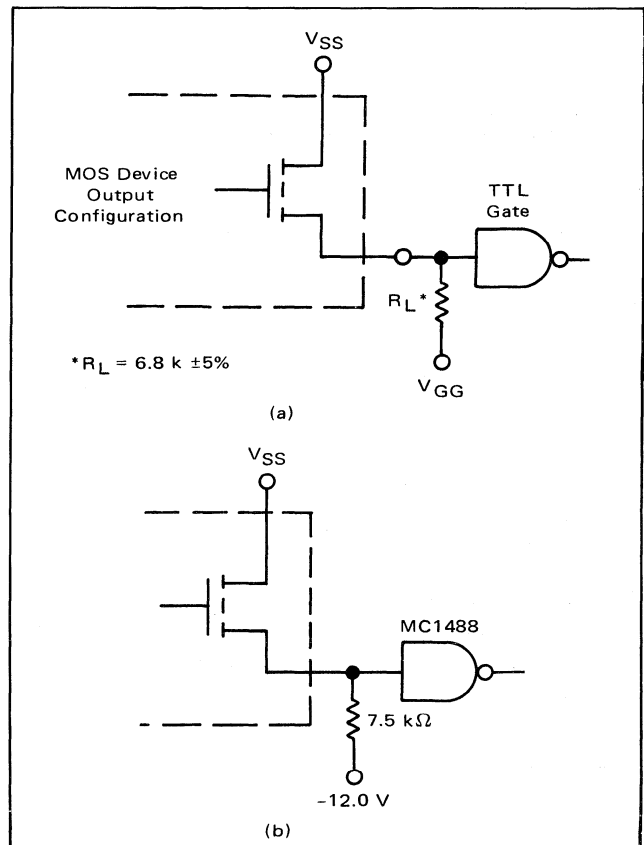FIGURE 28 — Transmitter and Receiver Input Configuration

FIGURE 29 — Transmitter and Receiver
TTL and MC1488 Interface

to meet the requirements of the RS232C specification by the addition of MC1488 line drivers and MC1489 line receivers. Generally the RS232C devices are required between chassis located on the same site. A 7.5 k ohm ±10% resistor to -12.0 V is required at the PMOS output to interface to the MC1488 driver as shown in Figure 29b. The MC1489 output is TTL compatible and can directly interface with any of the inputs of the transmitter or receiver.

The output configuration of the transmitter and receiver allows them to be used in different bussing configurations. For example, several transmitters can be tied together using one 6.8 k ohm pulldown resistor to send data to a receiver in a time share mode as shown in Figure 30. Likewise, the output of several receivers can be tied together using one 6.8 k ohm pulldown resistor for each common line to multiplex asynchronous data from several different sources as shown in Figure 31.

CONCLUSION

The terminal transmitter (MC2257 and MC2260) and terminal receiver (MC2259) have approximately a 35 to 1 reduction in part count over the conventional method of using MSI and SSI/TTL devices. Also, the power dissipation of the MOS transmitter and receiver is much less than that of a discrete TTL system. The Motorola terminal transmitter and receiver pair provide for both asynchronous and synchronous data transmission which is becoming a requirement for new terminal equipment designs. These two MIS/MOS parts should provide a new cost effective approach for the terminal manufacturer.
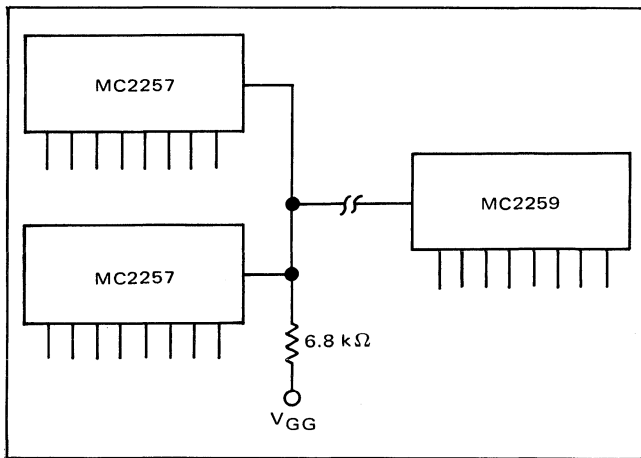

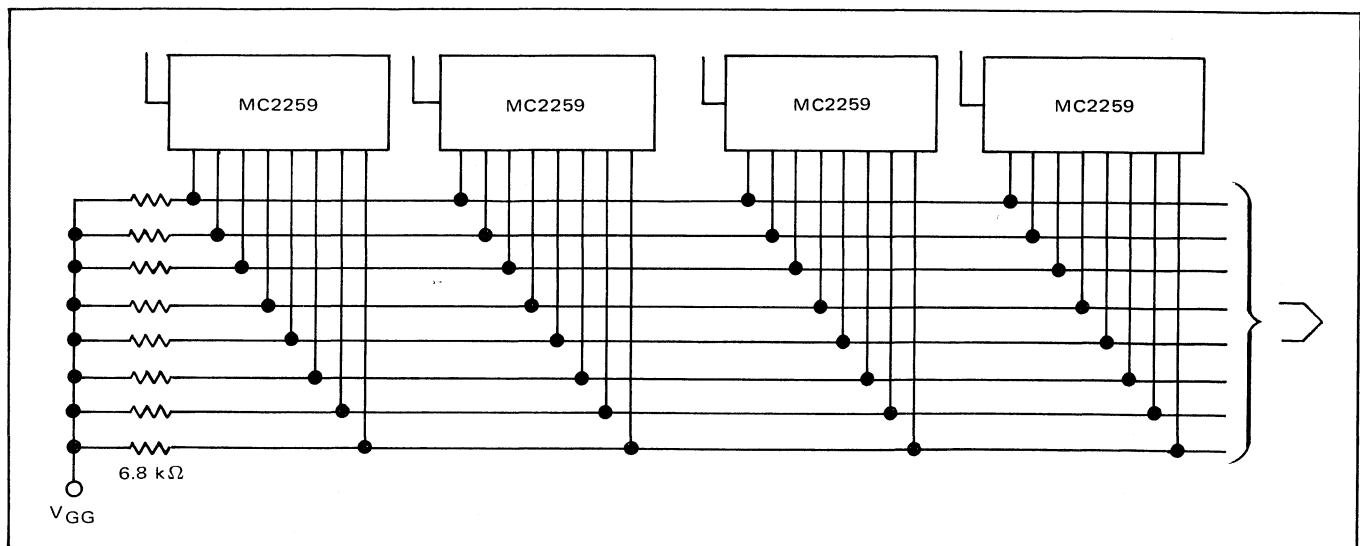FIGURE 30 — Transmitter Bussing Configuration

FIGURE 31 — Receiver Bussing Configuration